DESIGN AND ANALYSIS OF MODERN THREE-PHASE AC/AC POWER CONVERTERS FOR AC DRIVES AND UTILITY INTERFACE

A Dissertation

by

SANGSHIN KWAK

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2005

Major Subject: Electrical Engineering

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Approved as to style and content by:

Hamid A. Toliyat (Chair of Committee)	Shankar Bhattacharyya (Member)
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(Head of Department)

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ABSTRACT

Design and Analysis of Modern Three-Phase AC/AC Power Converters
for AC Drives and Utility Interface. (May 2005)
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Chair of Advisory Committee: Dr. Hamid A. Toliyat

Significant advances in modern ac/ac power converter technologies and demands of industries have reached beyond standard ac/ac power converters with voltage-source inverters fed from diode rectifiers. Power electronics converters have been matured to stages toward compact realization, increased high-power handling capability, and improving utility interface. Modern ac/ac power converter topologies with various control strategies have been introduced for the further improvements, such as matrix converters, current-fed converters, PWM rectifiers, and active power filters. In this dissertation, several new converter topologies are proposed in conjunction with developed control schemes based on the modern ac/ac converters which enhance performance and solve the drawbacks of conventional converters.

In this study, a new fault-tolerant PWM strategy is first proposed for matrix converters. The added fault-tolerant scheme would strengthen the matrix converter technology for aerospace and military applications. A modulation strategy is developed to reshape output currents for continuous operation, against fault occurrence in matrix converter drives.

This study designs a hybrid, high-performance ac/ac power converter for high power applications, based on a high-power load commutated inverter and a medium-power voltage source inverter. Natural commutation of the load commutated inverter is

actively controlled by the voltage source inverter. In addition, the developed hybrid system ensures sinusoidal output current/voltage waveforms and fast dynamic response in high power areas.

A new topology and control scheme for a six-step current source inverter is proposed. The proposed topology utilizes a small voltage source inverter, to turn off main thyristor switches, transfer reactive load energy, and limit peak voltages across loads. The proposed topology maximizes benefits of the constituent converters: high-power handling capability of large thyristor-based current source inverters as well as fast and easy control of small voltage source inverters.

This study analyzes, compares, and evaluates two topologies for unity power factor and multiple ac/ac power conversions. Theoretical analyses and comparisons of the two topologies, grounded on mathematical approaches, are presented from the standpoint of converter kVA ratings, dc-link voltage requirements, switch ratings, semiconductor losses, and reactive component sizes. Analysis, simulation, and experimental results are detailed for each proposed topology.

To my parents

and

my beloved wife, and my brother.

ACKNOWLEDGMENTS

I would like to express my heartfelt gratitude to my advisor, Dr. Hamid A. Toliyat, for his constant guidance and support through all my graduate study. His unlimited patience and kindness as well as insightful academic advice are very much appreciated. I was very fortunate to have worked with him over all these years.

I would like to acknowledge the members of my graduate study committee, Dr. Shankar Bhattacharyya, Dr. Mehrdad Ehsani, Dr. Ken Dykema, and Dr. Chanan Singh, for serving on my committee and for their invaluable advice and help. I also acknowledge Dr. Aniruddha Datta and Dr. Emil Straube for their assistance and help. My thanks are also extended to my fellow colleagues at the Advanced Electrical Machine and Power Electronics Lab at Texas A&M University.

I am deeply grateful to my parents and my brother for their endless love, support, and encouragement in all my endeavors. Especially, I am greatly indebted to my wife, Won-Young Kim, for her love and support. Without her sacrifice and love, I could not have completed this study.

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CHAPTER I

INTRODUCTION

1.1 AC/AC power conversion

Numerous modern industry applications, from low to high power areas, demand ac signals with adjustable amplitude and frequency. The variable ac signals are achieved through ac/ac power conversion from utility ac signal with fixed amplitude and frequency. Power converters transform frequency and amplitude of ac signal according to system requirements. The most traditional topology in today's off-the-shelf ac/ac power converter is a pulsewidth modulated voltage source inverter (PWM-VSI) with a front-end diode rectifier and a dc-link capacitor. The diode rectifier based PWM-VSI, shown in Fig. 1.1, has been the workhorse of the ac/ac power conversion for nearly 30 years [1]-[5]. This structure is comprised of two power-conversion stages and intermediate energy storage element. The diode rectifier converts the fixed ac signal in the utility to uncontrolled dc signal. The converted dc power signal is, then, stored in the dc-link capacitor. The PWM-VSI subsequently generates ac signals with arbitrary amplitude and frequency, using high-frequency switching operation. This configuration is based on indirect power conversion because the entire ac/ac conversion is performed through intermediate dc power conversion with dc-link between the two ac systems. The dc-link capacitor decouples two ac power conversion stages and ensures the independent control of two stages.

In recent years, significant advances in power semiconductor device technology, low-cost, high-speed control processors, and matured PWM algorithms have led to a number of modern ac/ac converter topologies. The trends for modern ac/ac power

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converters have been directed to improved utility interface with unity power factor, input current waveforms with minimized harmonics, compact-size converter implementation with low-volume, more integrating silicon structure with reduced passive components, and increased power handling capability with enhanced efficiency for high-power applications [5], [7]. Bearing them in mind, the diode rectifier based PWM-VSI system has several drawbacks caused by its topology and inherent limitation against the modern trends, notwithstanding its wide applications for industry.

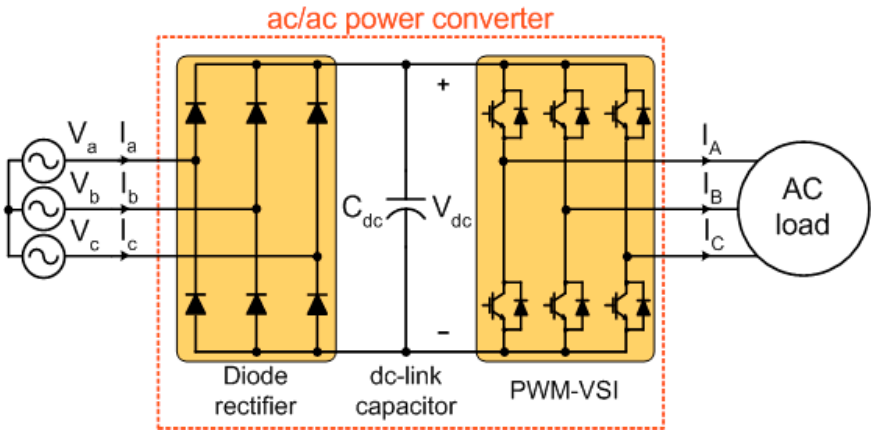


Fig. 1.1 Diode rectifier based PWM-VSI.

Typical disadvantages of the diode rectifier based PWM-VSI are the following:

1. Bulky system size and volume

   Massive and bulky dc-link reactive components are an inevitable part for the indirect power conversion to decouple two ac stages and store intermediate dc energy. The large electrolytic dc-link capacitor in the diode rectifier based PWM-VSI results in the bulky converter size and volume of the entire converter [12]. In addition, presence of the capacitor significantly limits the power converter to high temperature applications up to 300°C [15].

2. Limited power rating

   The output power level applicable to the diode rectifier based PWM-VSI is limited by the PWM-VSI with gate turn-off switches such as power MOSFETs or insulated

gate bipolar transistors (IGBTs). The PWM-VSI based on fast PWM switching operation, has shown intrinsic weakness for high-power areas, because of limited power rating of available gate-turn-off devices and substantial switching losses associated with hard switching operation resulting in heat dissipation issue. In addition, possibility of insulation failures and electromagnetic interference (EMI) due to high *dv/dt* stresses with fast switching operation is aggravated in high power applications [31].

3. Harmonic pollution in utility grid

   The harmonic pollution in the electrical utility is caused by the significant harmonic currents of the diode rectifier type utility interface [4]. Due to its uncontrolled operational characteristics, the diode rectifier produces distorted input current waveform with poor power factor. The harmonic utility currents by the rectifier yield an inefficient usage of electrical energy, equipment overheating, malfunction of solid-state equipment, interference with communication systems, and power quality degradation in distribution system [63], [64].

1.2 Modern ac/ac power converters

A matrix converter performs direct ac/ac power conversion from ac utility to ac load, with neither intermediate dc conversion nor dc energy storage elements [9]. Thus, the converter can be realized with greatly reduced size and volume in its structure, compared to the indirect ac/ac power converters grounded on dc-link components. Six-step current-fed converters based on thyristors are favorable in high power applications, because of no PWM operation, very reliable topologies with inexpensive high-power thyristors, and very low switching losses [27]. Controlled converter type utility interface such as a PWM voltage source rectifier (PWM-VSR), or an active power filter (APF) can be employed to solve the harmonic pollution problems of the uncontrolled diode

rectifier type interface [46], [50]. Table 1.1 summaries the problems and the alternative converters for the diode rectifier based PWM-VSI.

Table 1.1 Problems and solutions of diode rectifier based PWM-VSI.

Problems	**Sources**	**Alternative approaches**	**Modern converters**
Bulky system size And volume	DC-link capacitor	Direct ac/ac power conversion	Matrix converter
Output power Limitation	IGBT based PWM-VSI	Six-step current-fed converter	Thyristor-based current source inverter
Harmonic pollution in utility grid	Uncontrolled diode rectifier type utility interface	Controlled converter type utility interface	PWM-VSR and APF

1.2.1 Direct ac/ac power conversion

The matrix converter is a direct ac/ac power converter, which connects supply ac utility to output ac load through only controlled bi-directional switches. The output ac signals with adjustable magnitude and frequency are constructed by single-stage power conversion process. The direct ac/ac power conversion principle of the matrix converter leads to the distinct structure with no large dc-link energy storage components. Consequently, the matrix converter topology can be implemented with compact size and volume compared with the diode rectifier based PWM-VSI, where the dc-link capacitor generally occupies 30 to 50 % of the entire converter size and volume. This feature is very promising to the modern low-volume converter trend with high silicon integration. In addition to its compact design, it can draw sinusoidal input currents with unity displacement factor as well as sinusoidal output currents. The converter provides inherent bi-directional power flow capability so that load energy can be regenerated back

to the supply. Moreover, the matrix converter can operate at high temperature surroundings due to the lack of dc electrolytic capacitors, which is very vulnerable in high temperature. The converter also has a long lifetime with no limited-lifetime capacitors [13], [15].

A three-phase matrix converter is shown in Fig. 1.2. The converter configuration consists of nine bi-directional switches, which are arranged to connect any of input terminals *a*, *b*, and *c* to any of output lines *A*, *B*, and *C*. Modulation strategies for the bi-directional switches synthesize desired output voltages based on pieces of sinusoidal supply voltages, instead of constant dc voltages of the PWM-VSI.

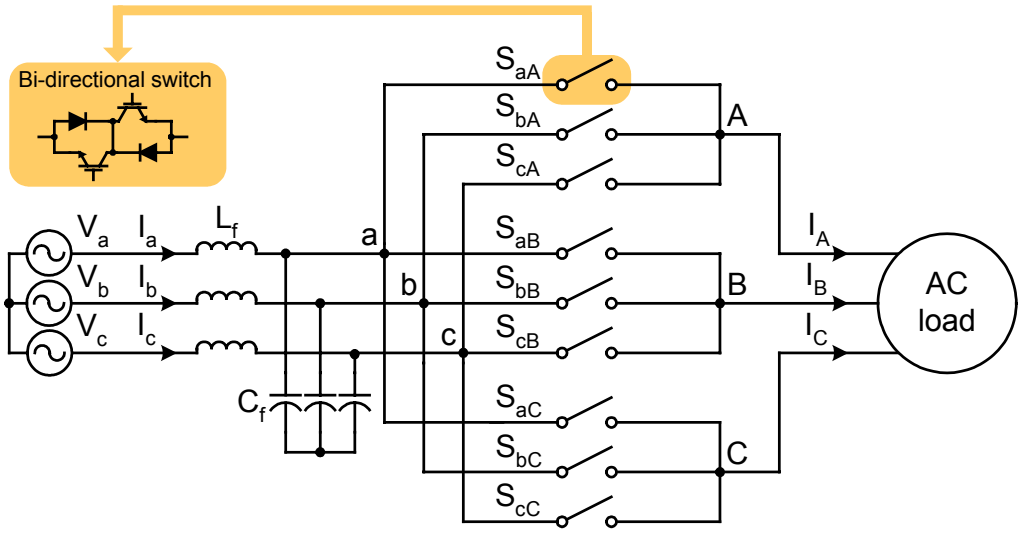


Fig. 1.2 Three-phase matrix converter.

1.2.2 Six-step current-fed converter

The converter power rating is closely tied to switching devices used in the converter topology. Even if gate-turn-off switching devices have been considerably improved, the switching characteristics are still far from being ideal, resulting in high switching losses from high-frequency hard switching operation. Figure 1.3 illustrates the power rating and operating frequency diagram of the switching devices [8]. Thyristors (or silicon-controlled-rectifier), invented by Bell Laboratory in 1956, possess the largest

power handling capability and are indispensable in high-power, low-frequency applications [2]. Power converter topologies with basis of thyristors have been traditionally used in high power utility system and multi-MW ac drive applications for which IGBT-based topologies with PWM operation are impractical due to device limitations. It appears that the dominance of thyristor in high power areas will not be challenged at least in the near future [4].

Thanks to thyristor characteristics and its soft switching operation, the thyristor-based topologies have performance merits including simplicity, easy control, high efficiency, reliability, cost effectiveness, and very low switching losses [25], [32], [40]. Moreover, because of its current-source inverter structure, it holds inherent advantages of CSI: 1) short-circuit protection: the output current is limited by the regulated dc-link current, 2) high converter reliability, due to the unidirectional nature of the switches and the inherent short-circuit protection, 3) instantaneous and continuous regenerative capabilities due to the controlled rectifier [32]. Because of all these features, the thyristor-based converters have been, so far, the favorable power converter topology in high power applications, with available switching devices at high power rating.

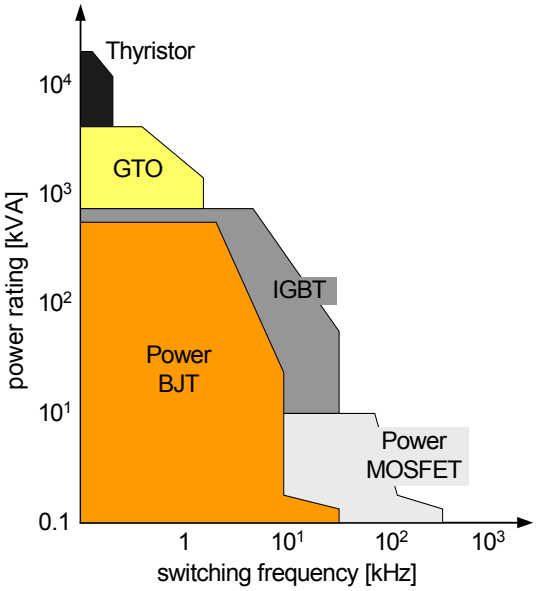


Fig. 1.3 Power-frequency diagram of power semiconductor devices.

A basic schematic configuration of a six-step current-fed converter based on thyristors is shown in Fig. 1.4. It consists of a three-phase controlled rectifier at input side and a current source inverter (CSI) at the output side with a dc-link inductor. The amplitude of the currents supplied to three-phase ac loads is controlled by adjusting the firing angle of the phase-controlled rectifier. The dc-link inductor reduces the current harmonics and ensures that the input of the CSI and hence, to the load appears as a current source. The thyristor-based inverter can control only the fundamental frequency of load currents by selecting the gating instances of thyristors. The thyristors in the inverter turn on and off only once per cycle of the load current, and consequently, the inverter operates in the six-step mode.

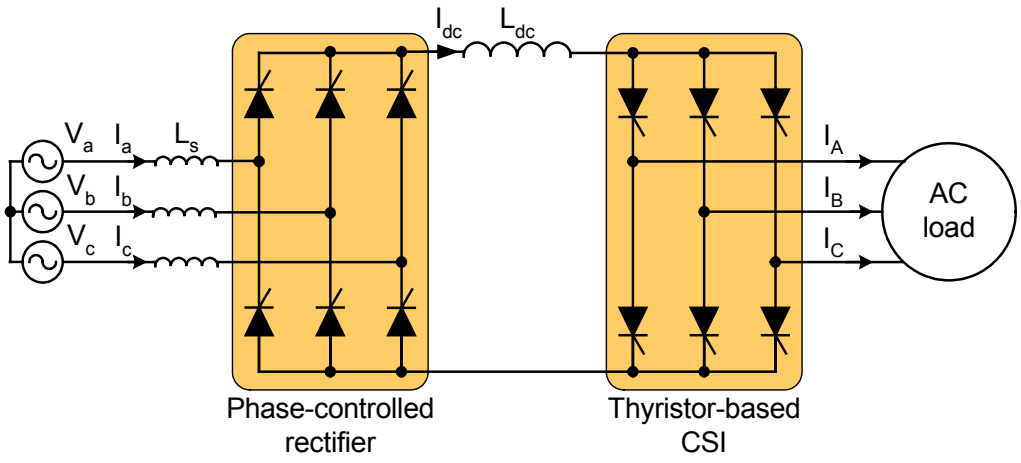
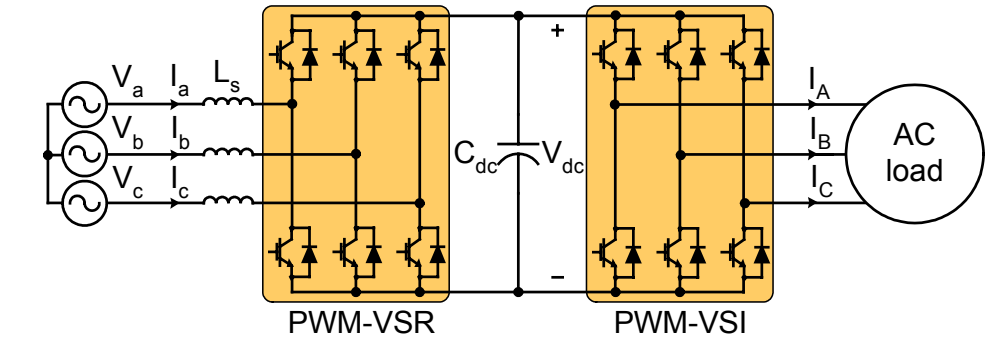


Fig. 1.4 Six-step current-fed converter.

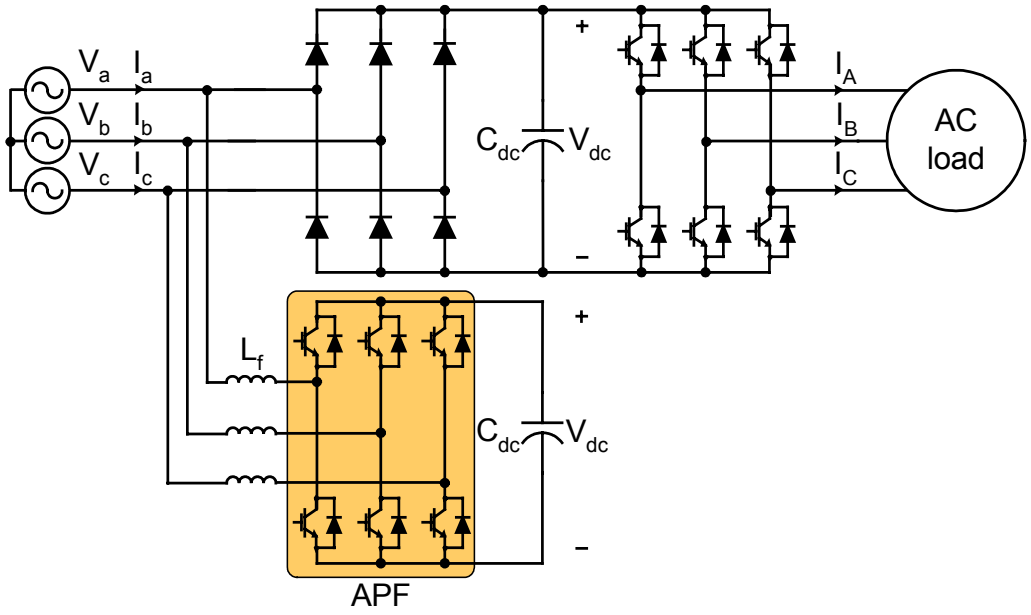
1.2.3 Controlled converter type utility interface

Increasing proliferation of power converters fed from the diode rectifiers results in increasing power quality concerns of utility distribution systems. This has led to standards to regulate utility power quality, such as IEEE-519 (American standard) and IEC EN 61000-3 (European standard). Numerous methods have been introduced from passive filter approaches through multiple-pulse rectifiers to converter type utility interface to solve the power quality degradation problems. Controlled converter type

utility interface achieves harmonic-free power system with active approach to shape supply current by power converters.



(a)



(b)

Fig. 1.5 Converter type utility interface (a) PWM voltage source rectifier topology (b) active power filter topology.

One topology is to replace the diode rectifier to the PWM voltage source rectifier (PWM-VSR) that has a built-in solution of input harmonic problems, shown in Fig. 1.5(a). The front-end PWM-VSR performs ac/dc power conversion as well as draws the

sinusoidal current waveforms from the utility. The other configuration is connecting the active power filter (APF) in parallel with the diode rectifier. The APF, illustrated in Fig. 1.5(b) injects both harmonic and reactive current components to the diode rectifier. Consequently, the utility can provide the only sinusoidal supply current with unity displacement factor. Although both converters perform unity power factor operation with sinusoidal input currents, the operational principles are quite different. The PWM-VSR is based on direct sinusoidal current generation, whereas the APF works on the principle of load harmonic compensation. As a consequence, the PWM-VSR deals with the real power, whereas the reactive and harmonic powers of the diode rectifier are supplied by the APF.

1.3 Review of previous works

In this section, operational features and technical difficulties of the above ac/ac power converters are briefly explained. The practical approaches of the converters are also reviewed with recent trends of the power converters.

1.3.1 Matrix converter

As the matrix converter structure is an array of switching devices connecting input source and output load, input and output sides are directly linked, in contrast with the diode rectifier based PWM-VSI separated by the dc-link capacitor. This aspect makes the modulation control of the matrix converter quite different and complicated, compared to other indirect ac/ac power converters. As a result, modulation techniques to control the matrix converter have been, last two decades, intensively researched and reported since the advent of Venturini's early method [9]. Two switching control strategies, Venturini method and Space Vector Modulation method (SVM) have been well established to obtain satisfactory input/output performances [9], [12].

1.3.1.1 Venturini modulation method

The Venturini modulation method, proposed by Venturini in 1980, is a direct transfer function approach to find relationship between input and output quantities. The output voltages of the matrix converter are determined by one of the input voltages according to connection status of the bi-directional switches. Therefore, instantaneous output voltages are synthesized by piecewise sampling of input voltages, so that mean output voltages averaged during switching period can track the desired sinusoidal voltage commands. As a result, three-phase output voltage set $\mathbf{V_{OUT}}$ can be represented by a transfer function matrix $\mathbf{T}$ and the input voltage set $\mathbf{V_{IN}}$ in (1.1). The transfer function matrix is composed of switching functions of the bi-directional switches.

$$\mathbf{V_{OUT}} = \mathbf{T} \times \mathbf{V_{IN}}$$

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} m_{aA} & m_{bA} & m_{cA} \\ m_{aB} & m_{bB} & m_{cB} \\ m_{aC} & m_{bC} & m_{cC} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{1.1}$$

where, m_{ij} denotes duty cycle of the corresponding bi-directional switch S_{ij} in Fig. 1.2 (i=a,b,c and j=A,B,C). As similar, the input currents of the matrix converter are constructed from the output currents, which are decided by the output voltages and load condition. From the input-output power balance (P_{in}=P_{out}), the low-frequency components of the input currents are found with the output currents and the transfer function matrix as

$$\mathbf{I_{IN}} = \mathbf{T^T} \times \mathbf{I_{OUT}} \tag{1.2}$$

where, $\mathbf{T^T}$ is the transpose matrix of $\mathbf{T}$. The matrix converter is fed by a voltage source in the input terminal and connected to an inductive ac load. Consequently, only one bi-directional switch in one output leg must close at any time, to avoid short-circuit in input side and open-circuit in inductive output terminal. This constraint can be expressed as

$$m_{aj} + m_{bj} + m_{cj} = 1, \qquad j \in \{\mathrm{A,B,C}\} \tag{1.3}$$

Finding PWM modulation algorithm of the matrix converter is now simplified to derive the closed form expression of the transfer function matrix $\mathbf{T}$ governing the bi-directional

switch control. In [9], Venturini presented a rigorous mathematical solution for the matrix **T** to generate sinusoidal output voltages and input currents. A modified modulation algorithm was developed to increase input/output voltage transfer ratio by adding zero-sequence third-harmonic voltage components in [10]. More sophisticated transfer functions have been proposed and derived to reflect some practical issues such as input voltage unbalance [11].

The Venturini modulation scheme is grounded on completely analytic and mathematical approach using the transfer function of input/output relationship. Notwithstanding straightforward grasp of the modulation concept, the Venturini method with somewhat inflexible style for practical implementation, is slowly losing its favor.

1.3.1.2 Indirect space vector modulation method

The indirect space vector modulation (indirect SVM), which was proposed by Borojevic in 1989, has been considered a standard modulation strategy of the matrix converter [12]. This modulation strategy is based on an equivalent model with the fictitious dc-link concept. From the standpoint of this modulation method, the matrix converter in Fig. 1.2 can be modeled as an equivalent circuit in Fig. 1.6, which is decoupled into a current source rectifier and a voltage source inverter. The equivalent model configuration is similar to a conventional back-to-back PWM-VSI structure, except lack of the dc-link capacitor. Thus, the space vector PWM (SVPWM) widely used in PWM-VSRs and PWM-VSIs can be independently dedicated to the rectifier and the inverter stage with same concept, but more complexity.

The rectifier stage constructs a virtual dc-link voltage U_{pn} from the input voltages, as well as maintains sinusoidal input currents. Based on the dc-link voltage built in the fictitious dc-link, the inverter stage generates output reference voltages with a balanced sinusoidal set by applying the SVPWM technique. Finally, the two modulation methods, independently derived from the two stages, are combined to create switching patterns of the entire matrix converter. The complete duty cycles of the matrix

converter are simply found as a product of the corresponding duty cycles calculated in the rectifier and the inverter stage of the equivalent model.

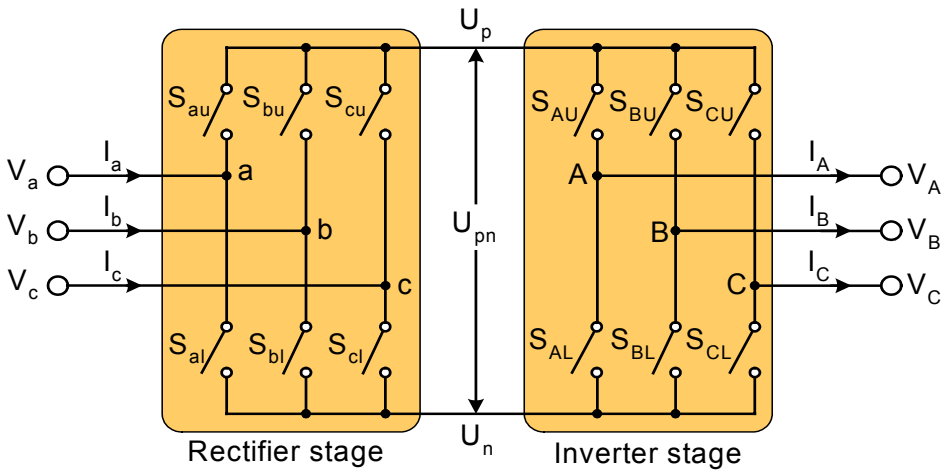


Fig. 1.6 Equivalent model of the matrix converter.

1.3.1.3 Recent trends

In spite of numerous merits presented in section 1.2.1, the industrial acceptance of the matrix converter has been held back because it is not suitable for use with standard loads on standard supplies due to its maximum input/output transfer ratio limited to 86%. In addition, many switching devices and gate drives, expensive system realization, increased complexity of control and current commutation, and sensitivity to input voltage disturbance have limited industrial interest in the matrix converter [13]. Therefore, the matrix converter has been expected to realize in practice for special applications where its advantages can offset the drawbacks, rather than general-purpose ac/ac power converter. Most potential practical implementation of the matrix converter has been considered aerospace, navy, and military applications, where reduced space and weight along with high-temperature operation are at a premium over cost and complexity penalty [15].

1.3.2 Thyristor-based current source inverter

The thyristor-based current source inverters have intrinsic drawbacks in association with the switching device, because latching characteristics is the basis of the thyristor switching operation. Once the thyristors are latched into on-state by the gate control signal, the gate terminals have no control ability to turn the devices off. The turn-off process must be accomplished by external circuits. To turn off the switching devices, external circuits must force the current through the thyristors below a holding current value, which is practically zero, for short period [3]. In other words, the device is required to be reverse-biased by the external circuit so that the current through the device falls down to zero. This feature ensures intrinsic soft switching operation of the devices. In fact, advantages of the thyristor-based CSI including cost effectiveness, ruggedness, very low switching losses, and simplicity have been gained at the expense of the turn-off ability [2]. Therefore, external devices and circuits are required to turn off the thyristors by applying reverse-biased voltage, as well as transfer reactive energies of inductive loads posterior to turning off the thyristors.

In general, the thyristor-based CSI can be classified with natural and forced commutation depending on commutation principle. Several types of the thyristor-based CSI have been proposed and developed with various external commutation methods and corresponding circuits.

1.3.2.1 Load-commutated current source inverter

One of the widely used thyristor-based CSIs is a load-commutated current source inverter, normally called a load commutated inverter (LCI). In the load commutated inverter utilizing the natural commutation, the devices are automatically off based on inverter terminal voltages, when the next thyristor in the sequence is gated on.

Figure 1.7 shows load commutation principle from thyristor T_1 to T_3, with T_2 on. The phase-controlled rectifier and the dc-link inductor are simplified as a dc current

source I_{dc}. The turn-off process of the off-going thyristor T_1 commences when the on-coming thyristor T_3 turns on. Turn-on time of the thyristor is appreciably shorter than its turn-off time [2]. As a result, the equivalent circuit in Fig. 1.7(b) is constructed during this commutation instant, t_{comm}. The off-going thyristor T_1 need be reverse-biased with negative voltage V_{T1}, which can be obtained by the load terminal A voltage V_A higher than V_B. Note that this terminal condition for the reverse-biased voltage of the off-going thyristor can be achieved if the inverter output currents lead the terminal phase voltages, as shown in Fig. 1.7(c). Therefore, the leading power factor in the inverter output terminal insures to turn off the thyristors and their natural commutation.

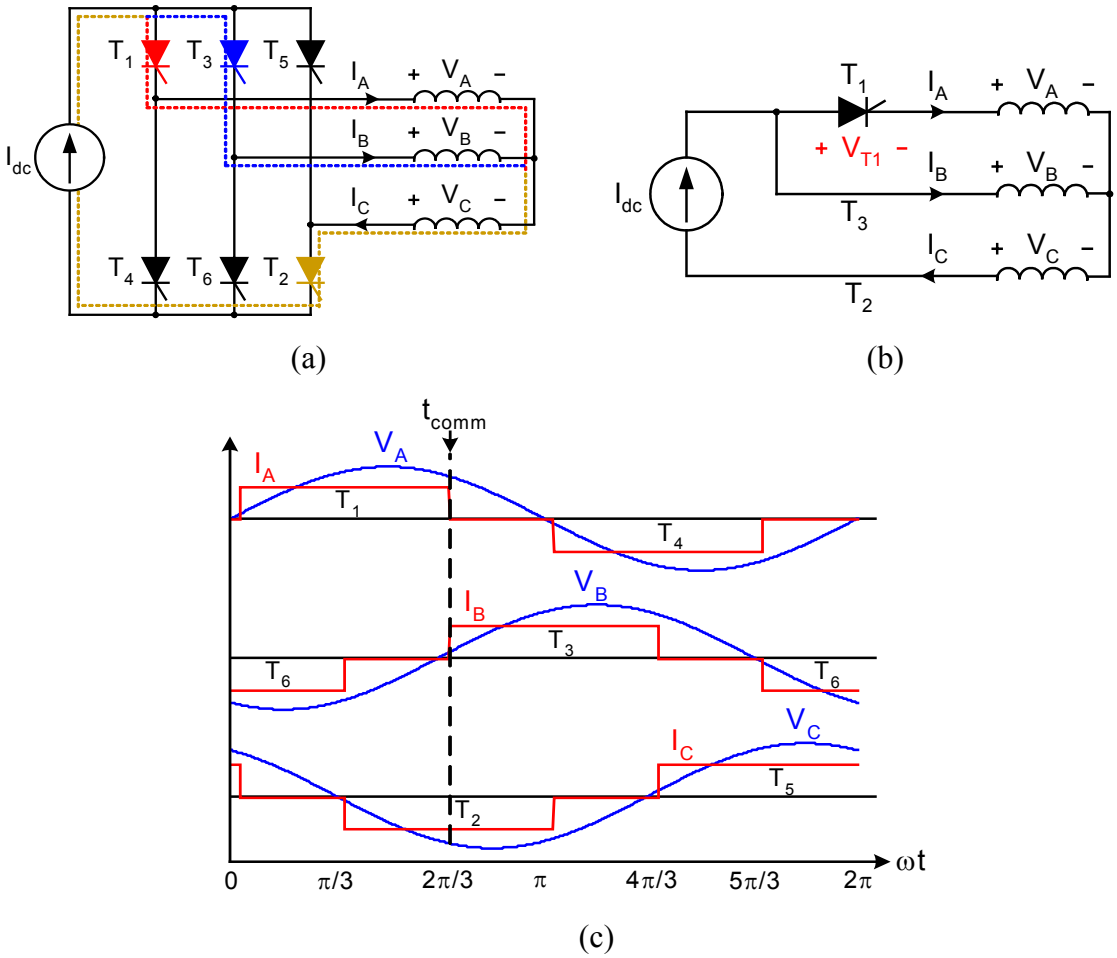


Fig. 1.7 Natural commutation from T_1 to T_3 (a) inverter diagram (b) equivalent circuit (c) output terminal voltage and current waveforms with leading power factor.

Because the overall commutation processes are *naturally* performed without any terminal voltage/current disturbance as far as the leading power factor is guaranteed, it is known as the natural commutation. This load commutated inverter has been typically applied to active loads capable of operating at leading power factor, such as synchronous machine loads [29], [33]. Because the commutation of the thyristors in the LCI is dependent on the load itself operating with leading power factor, the terminology of load commutated inverter has been originated.

However, this approach is not suited for inductive loads including induction motors, which must work at a lagging power factor. Therefore, external apparatuses are required to convert lagging power factor of inductive loads to leading power factor of the inverter terminal. A conventional method is to install additional output capacitors in parallel with the LCI [26]-[28]. A schematic configuration and vector diagram of the LCI using external capacitors are illustrated in Fig. 1.8. A vector diagram of Fig. 1.8(b) explicitly explains how the output capacitor generates a leading power factor at the LCI terminal. The output load current I_O in the inductive loads always lags the corresponding load voltage V_O with lagging angle θ, which depends on the inductive load characteristics. On the other hand, the output current of the LCI, I_{LCI} must lead the load voltage, V_O for successful thyristor commutation. The phase shift required from I_O to I_{LCI} is obtained by the output capacitors. The angle ϕ in Fig. 1.8(b) denotes the leading angle of the LCI terminal for safe commutation. Furthermore, the output capacitors serve two more functions: (1) They provide bypass current paths for the leakage currents of the inductive loads, so that leakage load currents can detour without overvoltage after turning off the thyristors. (2) The capacitors also smooth out the output current waveforms coming from the LCI.

This leading power factor allows thyristors in the LCI to commutate above critical frequency of inductive load currents. However, in low-frequency region, these output capacitors cannot make enough phase shift because the capacitor currents are too small due to high impedance of the capacitors [26], [27]. Since increasing the capacitance enough for the low-frequency region could yield unreasonably large capacitor, additional

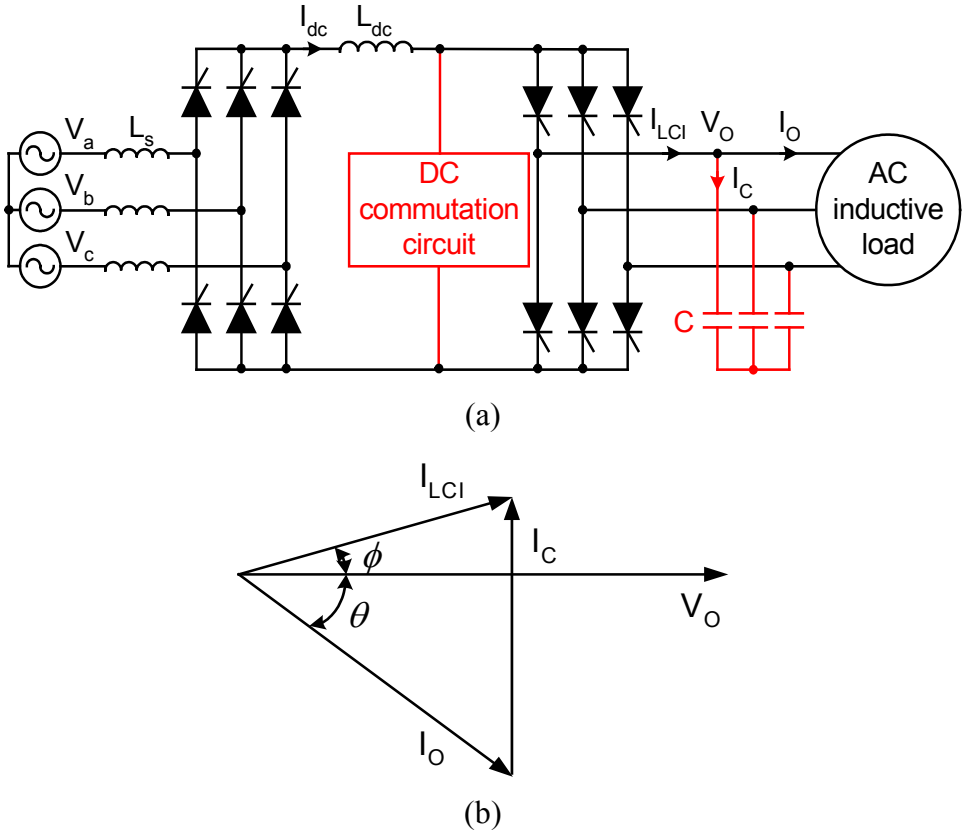


Fig. 1.8 Load commutated inverter (a) topology (b) vector diagram.

dc-commutation circuits are appended for low-frequency operation. The dc-commutation circuits are composed of high-power thyristors or GTO, diodes, and reactors [27]. The commutation circuits facilitate the commutation from one phase to another phase, by effectively bypassing the flow of dc-link current around the LCI. Consequently, switching devices and components with high power tolerance are utilized for the dc-commutation circuits, because entire load currents flow into the commutation circuits. This load commutated inverter with the output capacitors and the dc-commutation circuit has shown some drawbacks.

1. Since output ac capacitors should fully compensate the inductance effect in inductive loads in order to provide leading power factor, the required capacitor size must be increased in proportion to the power rating of the loads [26].
2. Output ac capacitors are not reliable, especially in high power application [25].

3. Resonance phenomena can be caused by the interaction between the output capacitor and the load inductance. These fundamental and harmonic resonance problems have seriously restricted the system performance [27].
4. Inherent instability in the high frequency region can be caused by the output capacitor [25].
5. The quasi-square-wave load current waveforms, rich in low order harmonics, produce considerable current harmonics, which can cause losses and heating in the loads. Furthermore, they can lead voltage spikes in the load inductances.

Approaches to reduce the output capacitor size were proposed by increasing the switching frequency of the LCI with inverter grade thyristors [26].

1.3.2.2 Forced-commutated current source inverter

A main difference between natural and forced commutation is that external circuits for the forced commutation work for only commutation periods of load currents. Note that the output capacitors of the LCI draw load currents at all times.

Figure 1.9 shows a conceptual circuit of a forced commutated current source inverter. A load current I_{LOAD} flows through a main thyristor T, and an auxiliary commutation switch S_{FC} in the forced commutation circuit keeps off at steady state. As a

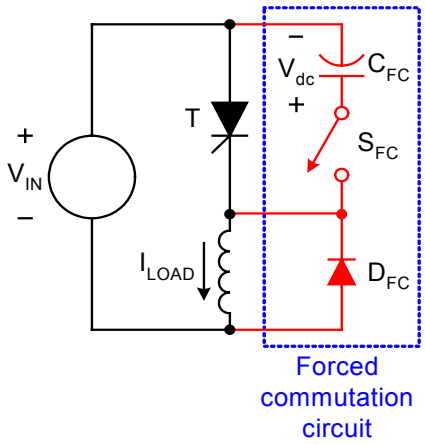


Fig. 1.9 Conceptual circuit of a forced commutated CSI.

result, the forced commutation circuit does not *appear* in the entire system during non-commutation periods. At commutation instants, S_{FC} turns on and the capacitor voltage V_{dc} imposes on the thyristor T in the reverse direction, turning it off. After T turned off, the load current, and hence the reactive load energy in the inductive load is delivered by the diode D_{FC} in the forced commutation circuit.

One widely used forced-commutated CSI is the auto-sequentially commutated inverter (ASCI) employing six commutation capacitors and six power diodes in Fig. 1.10. The most obvious advantage of the ASCI is to utilize the thyristors in the main circuit as the commutation switches. Therefore, the forced commutation can be achieved without any additional switching devices. As similar with the LCI, the thyristors in the ASCI conduct for 120°. Each off-going thyristor is automatically turned off when an on-coming thyristor is fired, because the commutation capacitors impress the reverse-biased voltage across the off-going thyristor. The diodes serve to isolate the commutation capacitors from the load and prevent the capacitor voltages from discharging after commutation. Despite of the autocommutating ability, the ASCI has some drawbacks caused by the commutation devices and operational principle, such as

1. A number of large, high-voltage ac capacitors are required.
2. High voltage stresses apply across the thyristors, the diodes, and load terminals [41].
3. Extra power losses incurred by the diodes located in the main load current paths are far from negligible, yielding reduced efficiency [1].
4. Commutation capacitor values are very sensitive to load parameters [43]-[45].
5. Upper operating frequency is limited because the ASCI needs long commutation delay time with capacitors [44], [45].

The commutation capacitors of the ASCI have been designed by compromising upper operating frequency range and high voltage stresses. Most of the ASCIs are practically accompanied with a voltage clamping circuit and an energy-transfer circuit, to overcome the limited frequency range and high voltage stresses. The voltage clamping circuit is used to reduce the voltage stresses while keep wide operating frequency range.

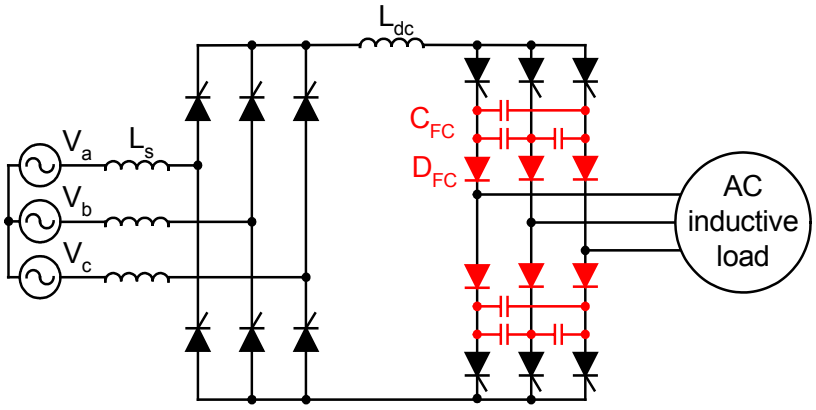


Fig. 1.10 Auto-sequentially commutated inverter.

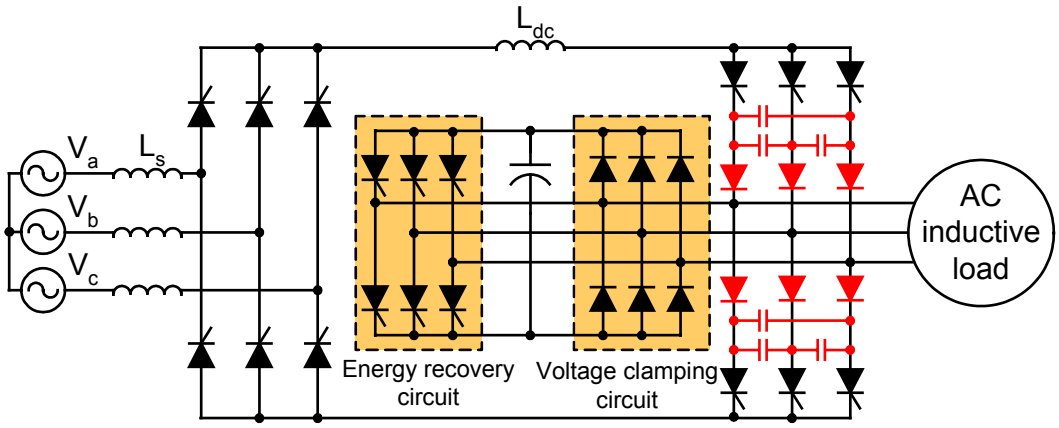


Fig. 1.11 Auto-sequentially commutated inverter with voltage clamping and energy recovery circuit.

The voltage clamping circuit, which usually consists of a three-phase diode rectifier followed by a dc capacitor, is connected in parallel with the ASCI output. Because each commutation process of the thyristors injects energy from the inductive load into the dc capacitor of the clamping circuit, the resultant energy in the dc capacitor needs to be dissipated or recovered. It is not desirable to dissipate the energy by connecting a discharging resistor in parallel with the dc capacitor, because the inverter efficiency would be seriously lowered [41]. Instead, an energy recovery circuit is added to transfer the energy stored in the dc clamping capacitor to the ac utility [42], [44], the

dc-link [43], or the load side [44], [4]. In [42], the reactive energy drawn from the load and stored in the dc clamping capacitor is returned to the utility side through the energy recovery circuit. In this kind of energy recovery circuit, another ASCI is required for the converter interfacing the dc clamping circuit and the utility. In addition, an isolated transformer is required between the utility side and the energy recovery circuit. Thus, the hardware cost and complexity is generally considered unacceptable. In [43], energy recovery circuits are designed to feed the recovered energy back to the dc-link side. This approach can cause undesired current ripple in the load side. In [44], the recovered energy is fed back to the load side by a proposed recovery circuit during commutation intervals. Figure 1.11 shows the ASCI topology with the voltage clamping circuit and the energy recovery circuit to load side.

Voltage clamping circuits and energy-transfer circuits have been realized with auxiliary thyristors, diodes, and reactors, as seen in Fig. 1.11. Thus, these circuits greatly increase the complexity of the inverter configurations, in conjunction with the commutation capacitors and the diodes. Moreover, the operational principles and control schemes are complex due to the additional circuits based on auxiliary thyristors, which cannot be self-turned off [44], [45].

1.3.2.3 Recent trends

Enormous changes have been occurred in the VSI topologies incorporated with the rapid development of controllable switching devices and consequent falling prices. However, the thyristor-based CSIs, such as the LCI and the ASCI, have remained basically unchanged from their original configuration, which utilizes capacitor commutation principles to turn off the thyristors. This capacitor commutation has placed main obstacle to the CSIs, because the cost of large ac capacitors with high-power ratings is escalating rather than decreasing [5]. Although the LCI and the ASCI have, at present and near future, found favor in high power applications, it is true that the converters operating on the basis of large capacitors slowly fade from the scene. One

important tendency in modern power converters is that price and size of active silicon-based switching devices are continuously reduced along with enhanced performance, whereas cost and size of passive components, such as capacitors, inductors, and transformers, are essentially constant [3]. Therefore, instead of the capacitor commutation, it would be good to develop a thyristor-based CSI integrated with recent VSI technology, which can maximize advantages of the two constituent converters: high-power capability of the thyristor-based CSI as well as easy and reliable control of small VSI with reduced cost.

1.3.3 PWM-VSR and APF

1.3.3.1 PWM-VSR

The PWM-VSR in Fig. 1.5(a) has been introduced as an advanced ac/dc power converter over primitive rectifiers such as the diode rectifier or the phase controlled rectifier. It converts the raw ac signal in the utility to controlled dc signal as well as improves the interaction with the utility grid, by directly forcing the input currents to be sinusoidal and in phase with the supply voltage. The operation of this topology is based on the boost power converter to shape the input currents at all times. Thus, the dc-link voltage should be always higher than input line voltage and the input inductor is an inevitable component for proper control. Two control loops are used to control the PWM-VSR: an outer voltage loop regulates the dc-link voltage and inner current loop shapes the input current to sinusoidal waveform with unity power factor. Because the PWM-VSR regulates both dc-link voltage and sinusoidal input current, ac/dc power conversion with high performance is realized through the PWM-VSR, compared to the diode rectifier with no dc-link control and distorted input current. In addition, this rectifier provides continuous regenerative capability. Despite all superiority over the diode rectifier, the main disadvantage of the topology is higher cost and increased complexity.

1.3.3.2 APF

The APF in Fig. 1.5(b) connects in parallel with a diode rectifier, and generates both harmonic and reactive power components required by the diode rectifier. The APF has basically the same circuit configuration as the PWM-VSR. The APF control is more complex than the PWM-VSR. This is mainly due to the operational principle to compensate load reactive and harmonic power components, which are highly distorted. In general, the cost of installing the APF is high and the APF suffers from difficulty in large-scale implementation [49]. Several approaches have investigated APF topologies and control strategies to reduce ratings [50]. In addition, a few papers have discussed study of the converter rating and the switch rating for the APF systems. In [47], a brief analysis for the converter kVA rating of the APF was presented based on a general nonlinear load. Nonetheless, the rating investigation is not complete since it did not consider the effect of an input filter inductor, which is an inevitable part for APF topologies with the boost configuration. In [59], switch rating analysis of the APF was proposed with a typical diode rectifier load.

1.3.3.3 Recent trends

Many applications in modern complex industry require multiple ac/ac power conversion, such as multi-drive applications for paper, textile, and oil-pumping areas. The demand of multiple inverter-load units and the high cost of the PWM-VSR have introduced single PWM-VSR feeding several dc/ac power converters, shown in Fig. 1.12. The multi-inverter concept has offered an attractive cost-effective approach because the cost and size of PWM-VSR can be shared by multiple inverter-load units [53]-[55]. In the topology of Fig. 1.12, the entire system can operate with unity power factor and sinusoidal utility current, as well as provide independent power control for two inverter-load units.

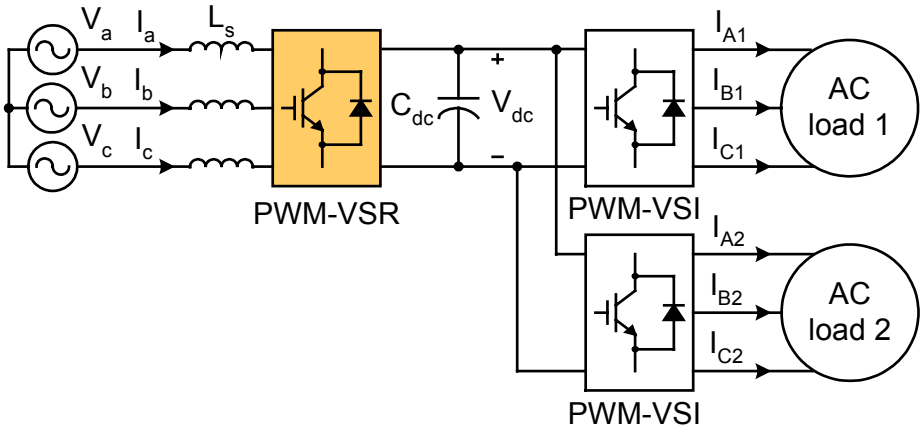


Fig. 1.12 PWM-VSR based topology with unity power factor and multiple ac loads.

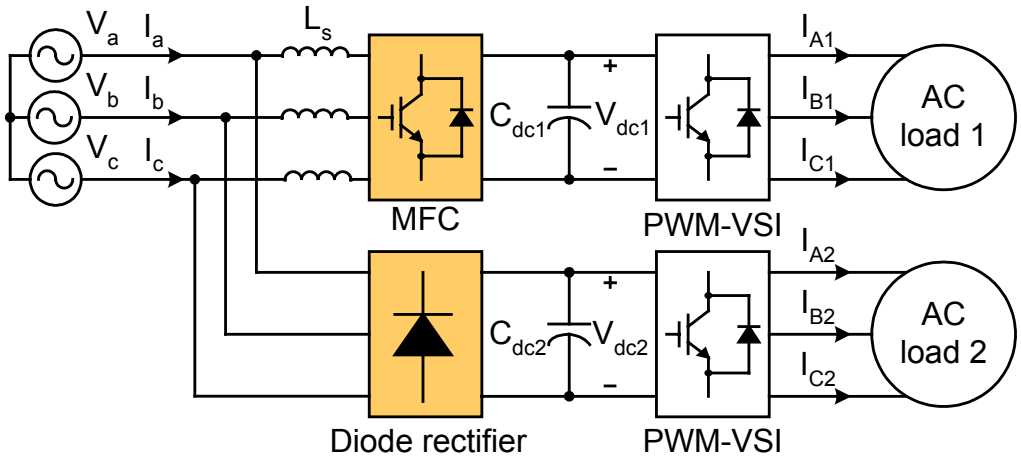


Fig. 1.13 MFC based topology with unity power factor and multiple ac loads.

The concept of the multiple inverter-load units with sinusoidal utility current can be also realized with the APF topology. In Fig 1.13, one inverter-load is fed from a diode rectifier, while the other unit is supplied by a PWM converter. Such a converter operates as a PWM-VSR to supply output power to its own inverter-load unit. At the same time, it functions as an APF by compensating harmonic and reactive power generated by the diode rectifier [50]-[52]. This topology has, in recent years, received an increased attention because it is expected to provide a more economic solution compared to the APF. Since this converter performs both the rectification and the active power filtering

functions, it is called a Multi-Function Converter (MFC) in this dissertation. Both topologies in Figs. 1.12 and 1.13 can operate at unity power factor with sinusoidal input currents on the utility side as well as achieve independent load controls on the output sides.

1.4 Research objectives

As discussed in this chapter, several modern ac/ac power converters have been introduced to improve shortcoming aspects of the diode rectifier based PWM-VSI and fulfil present industrial requests for converter circuits. The objective of this research work is to propose and analyze new approaches based on the ac/ac power converter topologies including the matrix converter, the thyristor-based current source inverter, the PWM-VSR, and the APF. This dissertation not only designs new topologies and control algorithms to enhance the performance of the ac/ac power converters, but also analyze and evaluate the topological systems.

The first objective of this research is to propose a fault-tolerant PWM strategy for matrix converter drives. Considering the converter reliability is particularly of great importance in the aerospace and military areas, the added fault-tolerant control would strengthen the matrix converter technology for its future applications. A modulation strategy of the matrix converter drives is developed to allow remedial function when one of the matrix converter drive legs is completely lost by any system fault. Based on a redefined converter structure, a fault-tolerant control method is derived to reshape output currents of two unfaulty phases for continuous operation. The proposed method allows improved system reliability with no hardware modification as well as no backup leg for a hardware redundancy, yielding no cost increase. Simulation and experimental results are presented to demonstrate the feasibility of the proposed fault-tolerant strategy for the matrix converter.

The second objective is to develop a hybrid converter system as high-performance ac/ac converter in high power applications. The proposed hybrid converter utilizes a combination of a load commutated inverter and a voltage-source inverter. The high-power LCI provides real power, while the medium-power VSI generates reactive and harmonic powers to a load. Both sinusoidal output currents and voltages are achieved through the hybrid converter in high power areas, where a standalone VSI cannot apply due to its power limitation. Furthermore, the VSI generates a leading power factor to allow natural commutation of the LCI. The LCI commutation is obtained based on active angle control of the VSI, rather than passive capacitor commutation and a forced dc-commutation circuit. While eliminating the capacitor commutation problems, the developed hybrid system ensures sinusoidal output current/voltage waveforms with high quality, fast dynamic response, and minimized VSI power rating through proposed control method. The feasibility of the proposed hybrid converter is verified by computer simulation and experimental results.

The third objective is to design a new six-step CSI topology utilizing small voltage source inverter as a forced-commutation circuit. Three tasks are performed by the VSI: 1) turning off thyristors in the CSI; 2) transfer of the reactive load energy through the VSI; 3) clamping the peak voltages across the load and the thyristors. Thus, single VSI with small power rating can completely replace a number of high-power ac capacitors, diodes, auxiliary thyristors in the forced-commutation circuit of the ASCI. The operational mode and control principle of the VSI is invented. The entire commutation process of the proposed CSI is very simple, easy, and reliable by the controllable switching devices of the VSI. The VSI operates only during commutation periods of the load currents and stops working over the non-commutation periods. Thus, the VSI with small power rating can be used for the proposed CSI system. The proposed system can take advantage of both constituent inverters: high-power capability of the thyristor-based CSI as well as simple and easy control of the VSI. Computer simulation and experimental results support the designed topology and control algorithm.

The final objective is to analyze, compare, and evaluate two topologies for unity power factor with sinusoidal utility currents and multiple ac/ac power conversions: single PWM-VSR feeding multiple inverter-load units, and the compound circuits of the diode rectifier and the MFC with their own inverter-load units. From input and output terminal point of view, two topologies in Figs 1.12 and 1.13, have shown equally satisfactory characteristics. Thus, the theoretical analyses and systematic comparisons of the two topologies, in detail, are presented from the internal standpoint: converter kVA ratings, dc-link voltage requirements, switch ratings, semiconductor losses and reactive component sizes.

1.5 Dissertation outline

This dissertation is categorized in six chapters in the following style. Chapter I presents the most primitive ac/ac power converter, and addresses its inherent drawbacks and limitations. The modern ac/ac converter topologies for the solutions are introduced with the operational principles and features. Then, reviews of the previous work for the modern ac/ac power converters and recent trends for the converters are, in brief, addressed along with practical problems. Finally, research objectives are presented.

In Chapter II, a fault-tolerant control strategy is proposed to improve system reliability of a matrix converter drive. Based on the redefined matrix converter structure, a new PWM modulation algorithm is developed to reshape output currents of the converter for continuous operation. Simulation and experimental results are presented to demonstrate the feasibility of the proposed scheme.

In Chapter III, a hybrid converter system is proposed by bringing a medium voltage-source inverter into a large load commutated inverter. The hybrid structure, control principle, and features are presented for high-performance ac/ac power converter in high power applications. The proposed hybrid converter is supported by the computer simulation and experimental results.

In Chapter IV, an advanced forced-commutation strategy using a small voltage source inverter is proposed for a thyristor-based current source inverter. The operational mode and control of the voltage source inverter is discussed. The feasibility of the proposed CSI topology, employing a small VSI as a commutation circuit, is verified with simulation and experimental results.

Chapter V presents two converters, the PWM-VSR and the MFC, for clean utility interaction and multiple ac/ac power conversion. This chapter, in detail, presents the theoretical analyses and systematic comparisons of the two converters, from converter kVA ratings, dc-link voltage requirements, switch ratings, reactive component designs point of views.

Chapter VI summarizes contributions of this research work in the several ac/ac power converters. Finally, some suggestions are included for future work.

CHAPTER II

FAULT-TOLERANT APPROACH TO THREE-PHASE MATRIX CONVERTER DRIVES*

2.1 Introduction

As explained in chapter I, the most potential implementations of the matrix converter have focused on aerospace, navy, and military applications where space, weight, and high temperature operation are critical issues over the cost and complex penalty [13], [15]. The reliability of the entire systems is particularly of great importance in these applications, where continuous operation of the system must be ensured with fault-tolerant strategy. The most common type of system faults is switch failure in one of the legs of the power converter, or alternatively, the loss of one of the load motor phases, resulting in one phase-opened circuit [16], [17]. Intelligent control methods for standard PWM-VSIs have been exploited to maintain the rotating magnetomotive force (MMF) by reformulating the remaining output current references after the opened-phase fault occurrence [16]-[18], [20]. In fact, the matrix converter is exposed to increased probability of switch failure due to its structure with numerous switching components. However, modulation methods for the matrix converter have been, so far, limited to generate three-phase balanced output voltages/currents, yielding a vulnerable control structure to the phase-loss faults. Little attention has been paid to fault-tolerant control strategy to improve the reliability of the matrix converter drives against the opened phase fault.

This chapter proposes a PWM modulation strategy, which can provide fault-tolerant operation for the matrix converter drive against sudden one phase failure. During normal condition, the output currents and voltages from the matrix converter are regulated with the three-phase balanced form by the conventional PWM modulation technique. In the event that one output phase of the matrix converter drive is open-circuited due to either switching semiconductor or motor phase failure, the matrix converter structure is modified by connecting a motor load neutral to a supply neutral. Based on two-phase structure resulted from the neutral connection, the proposed modulation strategy develops the two output currents shifted 60° phase with respect to each other, so as to maintain the rotating MMF and ensure disturbance free operation. The proposed method, along with only software modification, realizes the fault compensation scheme without any additional backup leg as a hardware redundancy. Thus, the proposed matrix converter drive can tolerate the opened-phase fault with least system cost increase to connect motor neutral. Therefore, the proposed scheme results in enhanced capability of the matrix converter drive applications in aerospace, navy, and military areas. The simulation and experimental results are shown to support the feasibility of the proposed fault-tolerant PWM modulation scheme.

2.2 Fault-tolerant configuration

2.2.1 Remodeling of output currents

In normal mode, the matrix converter regulates the output currents as a three-phase balanced set by

$$\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} = \begin{bmatrix} I_m \cos(\omega t + \phi) \\ I_m \cos(\omega t + \phi - 2\pi/3) \\ I_m \cos(\omega t + \phi + 2\pi/3) \end{bmatrix} \tag{2.1}$$

where, I_m, ω, and ϕ are the magnitude, frequency, and phase of the output current, respectively. The rotating MMF generated by the currents in (2.1) is

$$\begin{aligned} MMF_{tot}^{N} &= MMF_A + MMF_B + MMF_C \\ &= NI_A + NI_B e^{j120^\circ} + NI_C e^{j240^\circ} \end{aligned} \tag{2.2}$$

where, MMF_{tot}^{N} is the total MMF in the normal condition, and N is effective number of stator turns per phase in a motor load. Assuming that the phase C is suddenly open-circuited and the phase current I_C drops to zero, the resultant MMF in the fault case is

$$MMF_{tot}^{F} = NI_A^F + NI_B^F e^{j120^\circ} \tag{2.3}$$

where, MMF_{tot}^{F} is the total MMF in the fault condition, and I_A^F and I_B^F are the phase A and B currents after the fault, respectively. Output currents in two remaining phases to maintain the same MMF can be derived, from (2.2) and (2.3), as

$$\begin{aligned} I_A^F &= \sqrt{3} I_m \cos(\omega t + \phi - \pi/6) \\ I_B^F &= \sqrt{3} I_m \cos(\omega t + \phi - \pi/2) \end{aligned} \tag{2.4}$$

Likewise, the remaining output currents required after A and B phase failure can be found in the same manner. The current phasor diagrams for the post-fault conditions after one output phase failure are shown in Fig. 2.1. The output currents at A, B, and C phases in the fault condition are denoted with and I_A^F, I_B^F, and I_C^F, respectively.

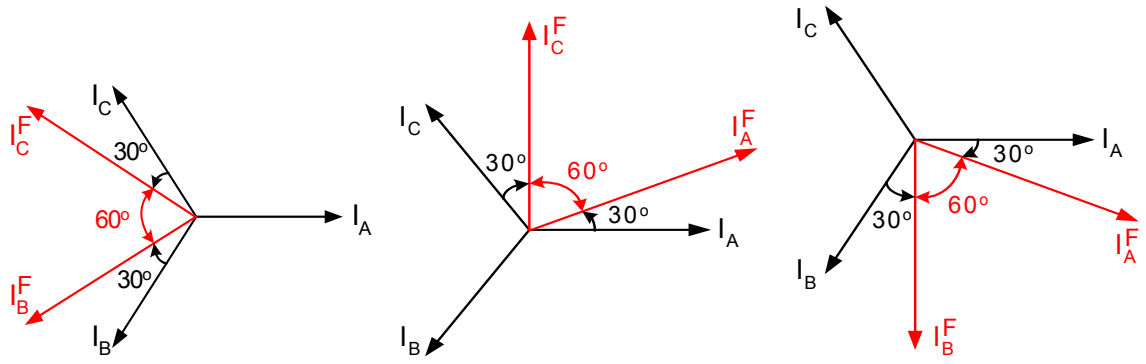


Fig. 2.1 Current phasor diagrams (a) phase A open fault (b) phase B open fault (c) phase C open fault.

Based on the above approach, the fault-tolerant strategy against one phase loss in the PWM-VSI drives has been well established by regulating the two unfaulty phase currents with the magnitude increased by a factor of $\sqrt{3}$ and phase shifted 30° away from the axis of the faulted phase [16], [18], [20]. The consequent asymmetric two-phase currents maintain a circular flux trajectory and the rotating MMF, resulting in the disturbance free operation of the load drives [16], [18]. Therefore, the fault tolerant control strategy requires the asymmetric two-phase current regulation on the unfaulty phases, distributed with 60° phase-shift with respect to each other. In the PWM-VSI topology with the dc-link capacitor, a neutral point of a motor load is connected to a midpoint of a dc-link, which is created by the use of two capacitors in Fig. 2.2. A connecting device TR_N, such as a TRIAC or a pair of back-to-back thyristors, is fired to link the motor neutral and the capacitor midpoint in fault occurrence. Grounded on the two split dc-link sources, the PWM-VSI provides two-phase operation with two remaining phases after open-phase fault.

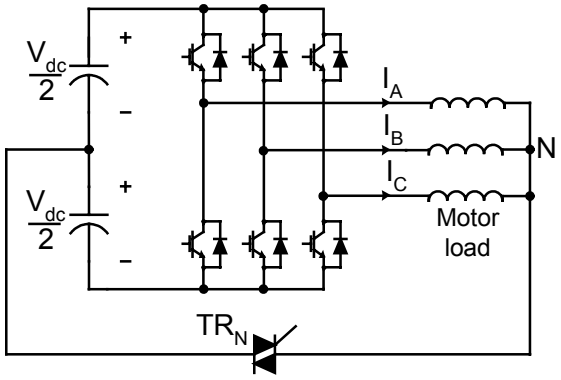
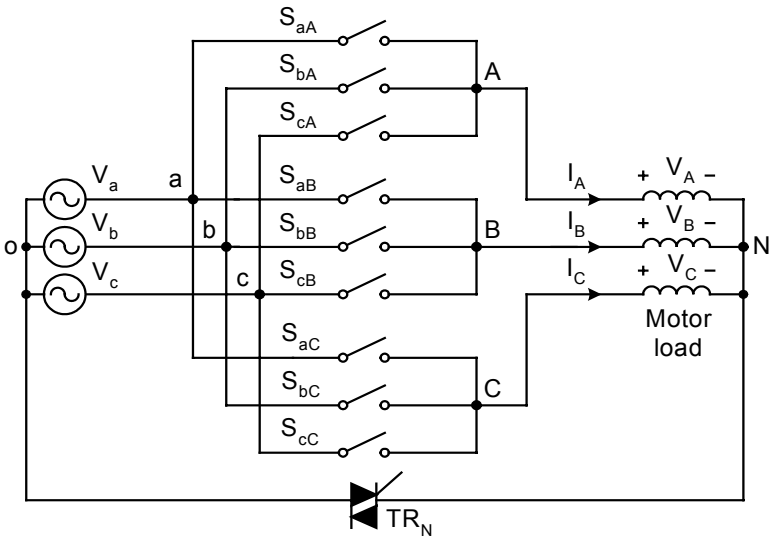


Fig. 2.2 Fault-tolerant topology of a PWM-VSI drive.

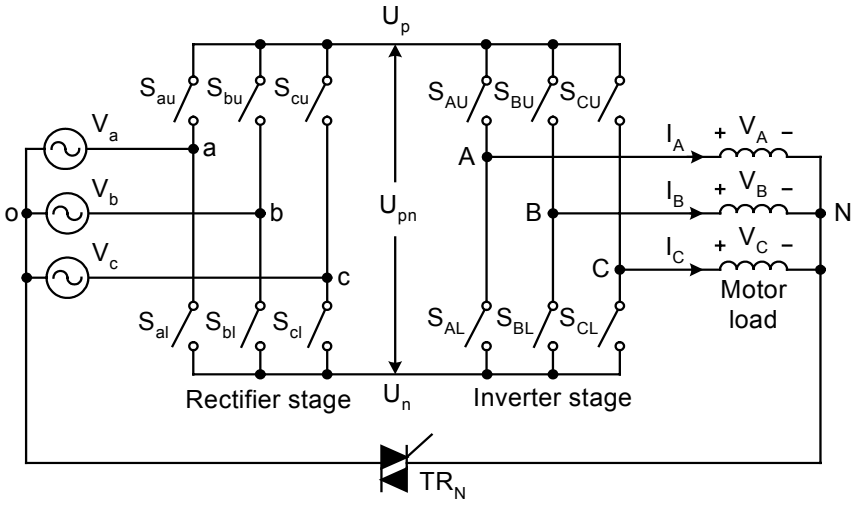
2.2.2 Normal mode

Figure 2.3(a) illustrates a three-phase matrix converter configuration with a connecting device between a motor neutral and a supply neutral. The connecting device TR_N, similarly, is used to modify the converter configuration after the opened-phase fault

occurrence. In normal condition, the connecting device is open, yielding no path between two neutrals. The equivalent model for the indirect space vector modulation is shown in Fig. 2.3(b), with the connecting device. The modulation scheme in the normal situations constructs single virtual dc-link voltage U_{pn} through the rectifier stage, and the inverter stage with the basis of the imaginary dc-link voltage generates the three-phase balanced output voltages and currents in (2.1), distributed with 120° phase angle.



(a)



(b)

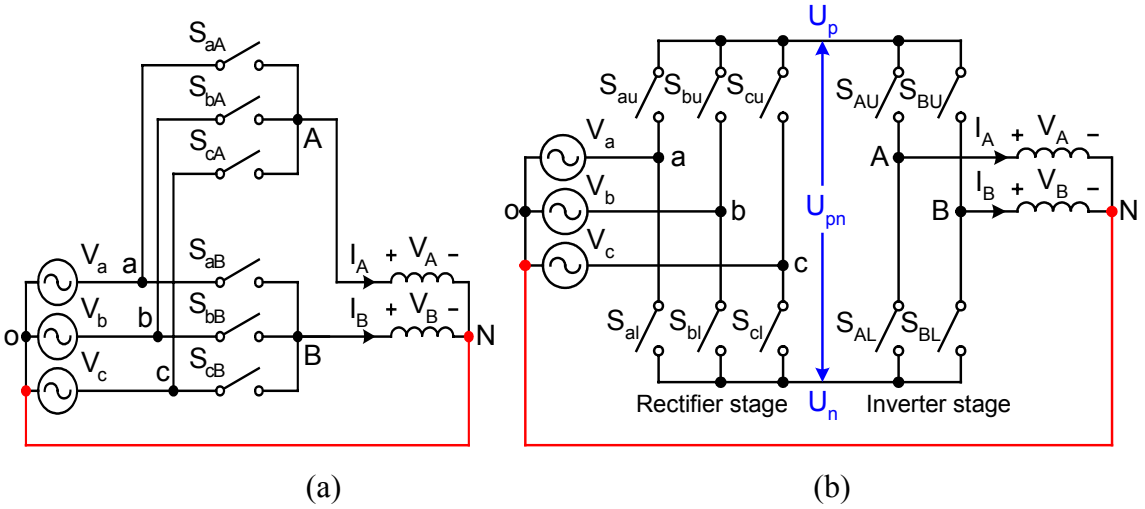
Fig. 2.3 Fault-tolerant matrix converter drive (a) converter circuit (b) equivalent model.

2.2.3 Faulty mode

Because the matrix converter topology has no dc-link capacitor, the motor neutral is connected to the supply neutral through the connecting device TR_N activated at the opened phase fault. Once the matrix converter drive detects the open-circuit fault of one output leg, the faulty leg is electrically isolated from the drive with removal of all switch commands on the phase, in order to eliminate its influence over the drive behavior [22]. Thus, the phase current on the faulty leg drops to zero. Furthermore, the connecting device is triggered on to interconnect the motor neutral to the supply neutral, leading to an asymmetric two-phase structure. After *C*-phase opened fault, the reconfigured matrix converter topology is obtained with isolation of the faulty *C* leg and interconnection of the neutral points, as shown in Fig. 2.4(a). The corresponding equivalent model is also depicted in Fig. 2.4(b).

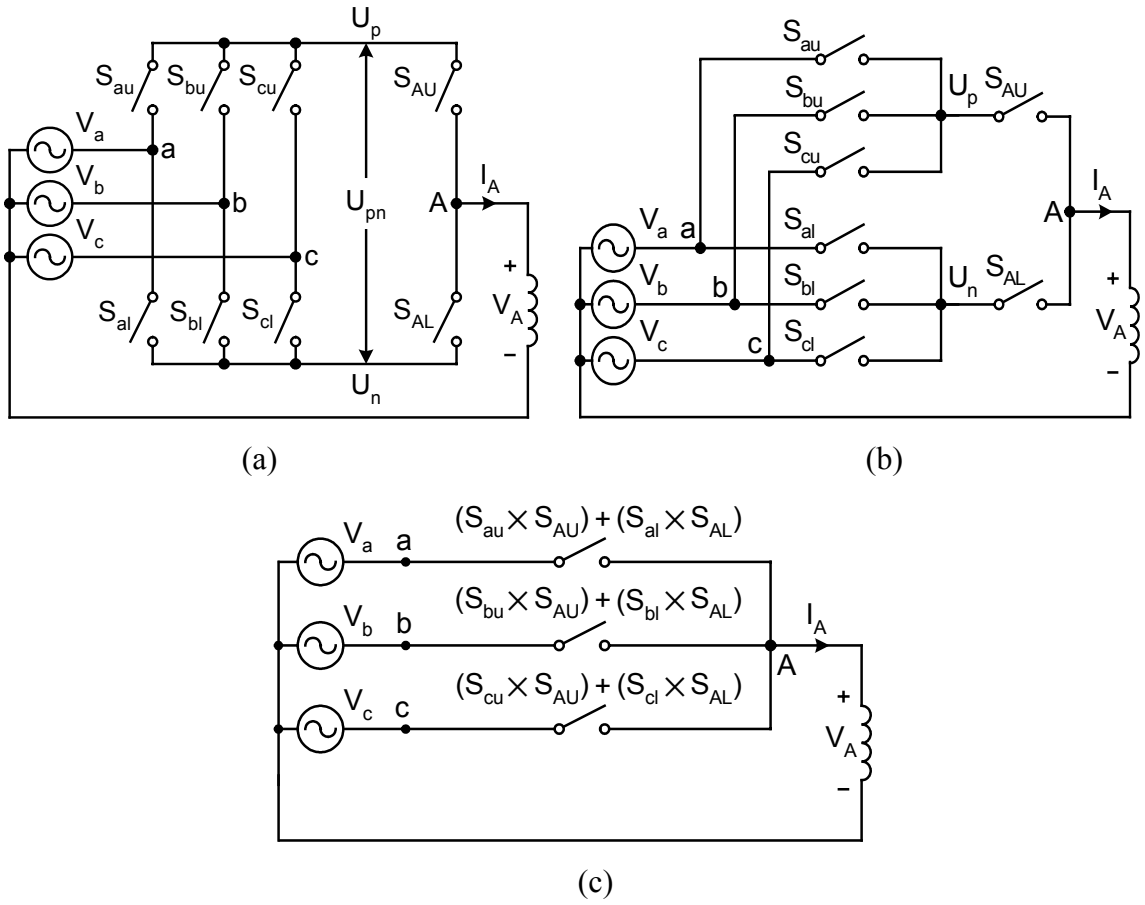
Figure 2.5 illustrates the transformation from the equivalent model with one output phase *A* to the matrix converter structure, with the motor neutral connected to the supply neutral [21]. The equivalent circuit of Fig. 2.5(a) is rearranged to Fig. 2.5(b). Then, Fig. 2.5(b) can be simplified to Fig. 2.5(c), which corresponds to the matrix converter configuration with single output phase. Because both the upper and the lower switches in one leg, for example, S_{AU} and S_{AL} cannot turn on simultaneously, the switch functions of the matrix converter can be derived by multiplying the switch functions of the rectifier and inverter stages. Adding one more output phase in Fig. 2.5(a) will bring one more output leg to the matrix converter in Fig. 2.5(c), yielding the matrix converter topology and its equivalent circuit in Fig. 2.4.

It should be noted that the inverter stage of the equivalent circuit in Fig. 2.4(b) must be supplied by two split dc-link sources to operate two remaining phases with the asymmetric two-phase operation, as the same case of the PWM-VSI based topology. Therefore, the rectifier stage must construct two equal imaginary dc-link voltages with respect to the supply neutral in the fictitious dc-link. Then, the inverter stage can perform SVPWM method for two-phase control based on the two dc-link voltages.



(a) (b)

Fig. 2.4 Topology after phase *C* loss (a) matrix converter (b) equivalent model.



(a) (b)

(c)

Fig. 2.5 Matrix converter and equivalent circuit with single output phase.

In this chapter, the fault tolerant strategy is derived considering opened-phase failure in the phase *C*. Similar approach can be applied for phase losses occurring in the phase *A* or *B*.

2.3 Proposed PWM modulation strategy

2.3.1 PWM strategy for rectifier stage

The main objective of the PWM modulation strategy in the rectifier stage is to create two virtual split dc-link voltages with equal amplitude in the dc-link, so that the two-phase operation can be performed in the inverter stage [23]. Figure 2.6 shows the rectifier stage with two conceptual capacitors split with respect to the motor neutral, which is connected to the supply neutral.

From Fig. 2.6, it is seen that the two virtual voltages in the fictitious dc-link should be constructed from the input voltages as

$$U_{po} = -U_{no} \tag{2.5}$$

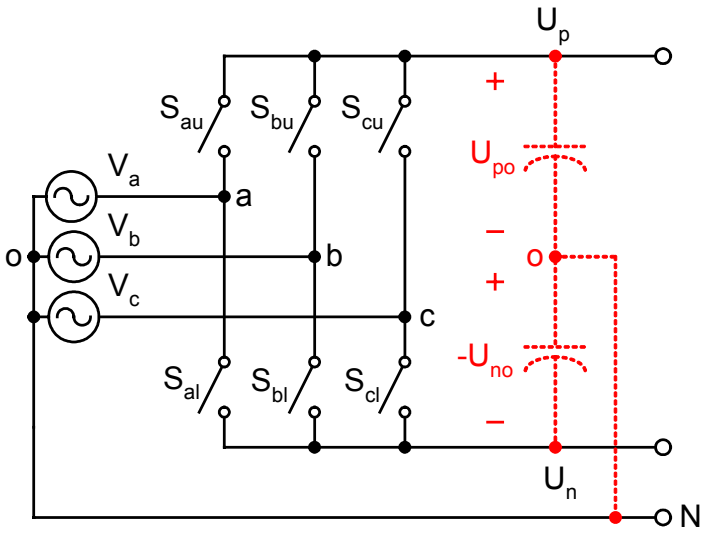


Fig. 2.6 Rectifier stage model for the fault-tolerant strategy.

Thus, the switches in the rectifier stage are modulated to generate the two voltages (U_p and U_n) with equal amplitude and opposite polarity with respect to the supply neutral, on the positive and negative rails of the fictitious dc-link. The input voltages are assumed to be a three-phase balanced set as

$$\begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix} = \begin{bmatrix} V_{im}\cos(\omega_i t) \\ V_{im}\cos(\omega_i t - 2\pi/3) \\ V_{im}\cos(\omega_i t + 2\pi/3) \end{bmatrix} \tag{2.6}$$

where, V_{im} and ω_i are the amplitude and the angular frequency of the input voltage, respectively. As shown in Fig. 2.7, twelve different rectifier sectors are defined, and at each sector, the input voltages are sorted according to their absolute magnitudes, as following:

$$\begin{aligned} U_{\max} &= MAX\left[|V_a|,|V_b|,|V_c|\right] \\ U_{mid} &= MID\left[|V_a|,|V_b|,|V_c|\right] \\ U_{\min} &= MIN\left[|V_a|,|V_b|,|V_c|\right] \end{aligned} \tag{2.7}$$

The 12 rectifier sectors fall into one of two possible categories and the PWM strategy of the rectifier stage can be generalized in each category.

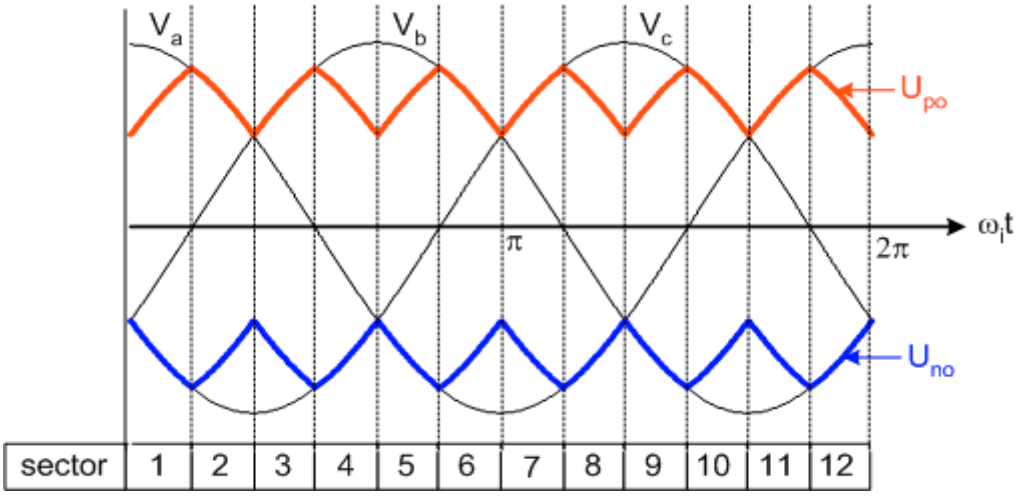


Fig. 2.7 Sector definition and two virtual dc-link voltages in the rectifier stage.

2.3.1.1 Category I: One input voltage is positive and two are negative

In this classification, the positive input voltage is assigned to U_{max}, and the two negative input voltages correspond to U_{mid} and U_{min}. The rules of switch control in this category are:

- The lower switch of the leg assigned to U_{mid} remains in conducting state.
- Two upper switches of two legs connected to U_{max} and U_{min} should be modulated.
- All other switches are turned off.

For example, in the rectifier sector 1 shown in Fig. 2.7, the input voltages on the phase *a*, *c*, and *b* are designated to U_{max}, U_{mid}, and U_{min}, respectively. The lower switch of the phase *c*, S_{cl} keeps on state during the entire sector 1. Thus, the voltage on the dc-link negative rail with respect to the supply neutral is given by

$$U_{no} = V_c \tag{2.8}$$

In the meantime, two upper switches of the phase *a* and *b*, S_{au} and S_{bu}, are modulated to create the proper voltage on the dc-link positive rail from the input voltages V_a and V_b. The local-average voltage in the dc-link positive rail with respect to the supply neutral is

$$U_{po} = d_\delta V_a + d_\gamma V_b \tag{2.9}$$

where, d_δ and d_γ are the duty cycles of the modulating switches related to U_{max} and U_{min}, respectively. In the rectifier sector 1, d_δ and d_γ correspond to the duty ratios of S_{au} and S_{bu}, respectively. The duty cycles of the modulation switches are constrained by

$$d_\delta + d_\gamma = 1 \tag{2.10}$$

The modulation functions of the switches S_{au} and S_{bu} are determined to synthesize the two equal split dc-link voltages. Substituting (2.6), (2.8), (2.9), and (2.10) into (2.5), the duty cycle d_δ can be obtained

$$d_\delta = \frac{\cos \varphi_i}{\sqrt{3}\cos(\varphi_i + \frac{\pi}{6})} \tag{2.11}$$

where, $\varphi_i = \omega_i t$. All other switches are turned off. The local-average values of U_{po} and U_{no} in this rectifier sector are

$$\begin{aligned} U_{po} &= -V_c \\ U_{no} &= V_c \end{aligned} \tag{2.12}$$

2.3.1.2 Category II: Two input voltages are positive and one is negative

In this category, the negative input voltage becomes U_{max}, and the two positive voltages correspond to U_{mid} and U_{min}. The switching rules in this category are:

- The upper switch of the leg connected to U_{mid} maintains on state.
- Two lower switches of two legs associated with U_{max} and U_{min} are modulated.
- As before, all other switches are open.

In the rectifier sector 2 as an example of this group, the input voltages on the phase *c*, *a*, and *b* correspond to U_{max}, U_{mid}, and U_{min}, respectively. The upper switch of the phase *a*, S_{au} keeps on state. As a result, the dc-link positive rail voltage with the respect to the supply neutral is given by

$$U_{po} = V_a \tag{2.13}$$

Meanwhile, the lower switches connected to the voltages U_{max} and U_{min}, S_{cl} and S_{bl} are modulated to construct the local-average voltage on the dc-link negative rail given by,

$$U_{no} = d_\delta V_c + d_\gamma V_b \tag{2.14}$$

where, d_δ and d_γ are the duty cycle of the switch S_{cl} and S_{bl}, respectively. As before, the duty cycle of d_δ is found by (2.5), (2.6), (2.10), (2.13), and (2.14), as

$$d_\delta = \frac{\cos(\varphi_i - \frac{\pi}{3})}{\sqrt{3}\cos(\varphi_i - \frac{\pi}{2})} \tag{2.15}$$

The local-average values of the two voltages U_{po} and U_{no} are given, in the rectifier sector 2, by

$$U_{po} = V_a$$
$$U_{no} = -V_a \tag{2.16}$$

Based on the above derivation, the modulating switches and their duty cycles can be decided in all rectifier sectors. The on switches, the modulation switches, and the duty cycles are shown in Table 2.1, from the sector 1 to 6. The local-average values of the two virtual dc-link voltages can be finally expressed as

$$U_{po} = U_{mid}$$
$$U_{no} = -U_{mid} \tag{2.17}$$

Therefore, it is seen that the proposed PWM modulation scheme in the rectifier stage builds the two virtual dc-link voltages with equal amplitude, U_{mid}, in the fictitious dc-link. The two local-average voltages U_{po} and U_{no} are also illustrated in the Fig. 2.7.

Table 2.1 Conduction switches and duty cycle values of rectifier stage.

Rectifier sector	U_{max}	U_{mid}	U_{min}	Modulating switches		On switch	d_δ value
				d_δ	$d_\gamma (=1-d_\delta)$		
1	V_a	$-V_c$	$-V_b$	S_{au}	S_{bu}	S_{cl}	$\frac{\cos\varphi_i}{\sqrt{3}\cos(\varphi_i+\pi/6)}$
2	$-V_c$	V_a	V_b	S_{cl}	S_{bl}	S_{au}	$\frac{\cos(\varphi_i-\pi/3)}{\sqrt{3}\cos(\varphi_i-\pi/2)}$
3	$-V_c$	V_b	V_a	S_{cl}	S_{al}	S_{bu}	$\frac{\cos(\varphi_i+2\pi/3)}{\sqrt{3}\cos(\varphi_i+5\pi/6)}$
4	V_b	$-V_c$	$-V_a$	S_{bu}	S_{au}	S_{cl}	$\frac{\cos(\varphi_i-2\pi/3)}{\sqrt{3}\cos(\varphi_i-5\pi/6)}$
5	V_b	$-V_a$	$-V_c$	S_{bu}	S_{cu}	S_{al}	$\frac{\cos(\varphi_i+\pi/3)}{\sqrt{3}\cos(\varphi_i+\pi/2)}$
6	$-V_a$	V_b	V_c	S_{al}	S_{cl}	S_{bu}	$\frac{\cos\varphi_i}{\sqrt{3}\cos(\varphi_i-\pi/6)}$

2.3.2 PWM strategy for inverter stage

Because the rectifier stage has generated the two virtual dc voltage sources with magnitude U_{mid} in the dc-link, the inverter stage becomes equal to a four switch inverter configuration supplying two-winding machines with the motor neutral connected to the fictitious dc-link midpoint. Figure 2.8 illustrates the equivalent circuit of the inverter stage with the imaginary dc-link voltages created by the rectifier stage. Therefore, conventional space vector modulation used for two-phase machine controls can be directly applied to the inverter stage [19].

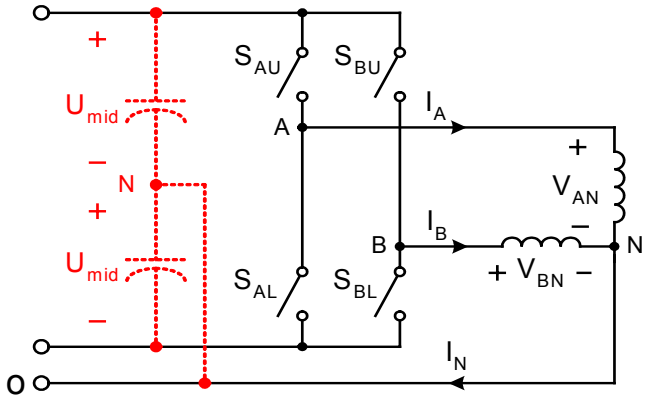


Fig. 2.8 Equivalent circuit of the inverter stage.

The space vector modulation technique is implemented based on the $\alpha\beta$ stationary reference frame using the transformation equation as

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} x_A \\ x_B \\ x_C \end{bmatrix} \tag{2.18}$$

The quantity x can be either output voltage or output current vector. It is assumed that the upper switches S_{AU} and S_{BU} have the binary value ‘1’ and ‘0’ in a closed state and an

open state, respectively. The lower switches S_{AL} and S_{BL} have the complementary value of their upper switches. Four possible combinations of the conducting switch states generate four different basis vectors in the $\alpha\beta$ plane, as illustrated in Table 2.2. The space vector diagram in the $\alpha\beta$ plane, which is split into two sectors, is shown in Fig. 2.9.

Table 2.2 Switching combination and basis vectors in the inverter stage.

S_{AU}	S_{BU}	Basis vectors
0	0	$V_1 = \sqrt{6} \cdot U_{mid} \cdot e^{-j2\pi/3}$
1	0	$V_2 = \sqrt{2} \cdot U_{mid} \cdot e^{-j\pi/6}$
1	1	$V_3 = \sqrt{6} \cdot U_{mid} \cdot e^{j\pi/3}$
0	1	$V_4 = \sqrt{2} \cdot U_{mid} \cdot e^{j5\pi/6}$

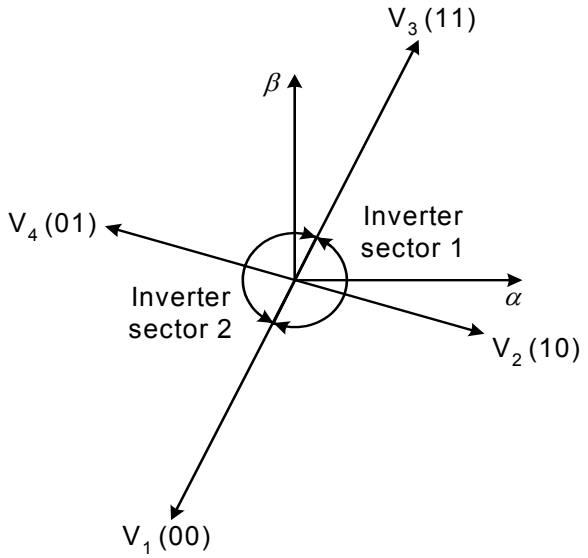


Fig. 2.9 Space vector diagram for PWM strategy in the inverter stage.

The effect of zero-sequence voltage component on the space vector analysis is assumed to be negligible because the zero-sequence circuit consists of very small impedance with

no speed voltage term in typical ac machines [20]. The desired voltage vector $V_{out}^{*}(=V_{\alpha}^{*}+jV_{\beta}^{*})$ is synthesized by impressing three basis vectors during required time intervals within one sampling length T_s. In the inverter sector 1, the reference voltage vector is composed by weighted time averages of the vectors V_1, V_2, and V_3 as,

$$V_{out}^{*}T_s = V_1 t_\alpha + V_2 t_\beta + V_3 t_0 \tag{2.19}$$

The time weights of the basis vectors are restricted to

$$T_s = t_\alpha + t_\beta + t_0 \tag{2.20}$$

The duty cycles are given by [19]

$$\begin{aligned} d_\beta &= \frac{t_\beta}{T_s} = \frac{1}{2\sqrt{2}U_{mid}}\left(\sqrt{3}V_\alpha^{*} - V_\beta^{*}\right) \\ d_\alpha &= \frac{t_\alpha}{T_s} = \frac{1}{2}\left(1 - \frac{1}{2\sqrt{6}U_{mid}}\left(V_\alpha^{*} + \sqrt{3}V_\beta^{*}\right) - d_\beta\right) \\ d_0 &= \frac{t_0}{T_s} = 1 - d_\alpha - d_\beta \end{aligned} \tag{2.21}$$

In the sector 2, the basic vectors V_3, V_4, and V_1 are employed to create the reference output voltage.

2.3.3 Combination of two stages

The complete matrix converter modulation can be obtained by multiplying the corresponding duty cycles obtained by the rectifier and the inverter stages, as the case of conventional matrix converter. The switching sequence shown in Fig. 2.10 assures the complete matrix converter operation from the rectifier stage and the inverter stage switching. The duty cycles of the matrix converter are found by multiplying the duty cycles as

$$\begin{aligned} &d_{\delta\alpha} = d_\delta \cdot (d_\alpha / 2) \quad , \quad d_{\delta\beta} = d_\delta \cdot (d_\beta / 2) \\ &d_{\gamma\alpha} = d_\gamma \cdot (d_\alpha / 2) \quad , \quad d_{\gamma\beta} = d_\gamma \cdot (d_\beta / 2) \\ &d_0 = 1 - (d_{\delta\alpha} + d_{\delta\beta} + d_{\gamma\alpha} + d_{\gamma\beta}) \end{aligned} \tag{2.22}$$

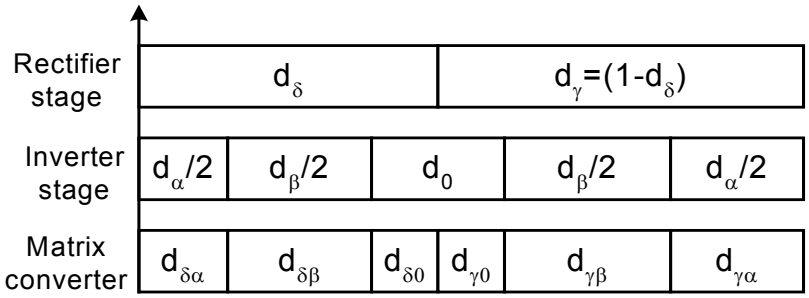


Fig. 2.10 PWM switching sequences for matrix converter.

Table 2.3. Switching states and duty cycles of the matrix converter after *C*-phase failure.

Rectifier sector	Inverter sector	DC voltages U_{po} U_{no}	Inverter switches S_{AU} S_{BU}	Output voltages V_{AN} V_{BN}	Duty cycle	Matrix converter Switching states S_{aA} S_{bA} S_{cA} S_{aB} S_{bB} S_{cB}
1	1	V_a V_c	0 0	V_c V_c	$d_{\delta\alpha}$	0 0 1 0 0 1
		V_a V_c	1 0	V_a V_c	$d_{\delta\beta}$	1 0 0 0 0 1
		V_a V_c	1 1	V_a V_a	$d_{\delta 0}$	1 0 0 1 0 0
		V_b V_c	1 1	V_b V_b	$d_{\gamma 0}$	0 1 0 0 1 0
		V_b V_c	1 0	V_b V_c	$d_{\gamma\beta}$	0 1 0 0 0 1
		V_b V_c	0 0	V_c V_c	$d_{\gamma\alpha}$	0 0 1 0 0 1
	2	V_a V_c	1 1	V_a V_a	$d_{\delta\alpha}$	1 0 0 1 0 0
		V_a V_c	0 1	V_c V_a	$d_{\delta\beta}$	0 0 1 1 0 0
		V_a V_c	0 0	V_c V_c	$d_{\delta 0}$	0 0 1 0 0 1
		V_b V_c	0 0	V_c V_c	$d_{\gamma 0}$	0 0 1 0 0 1
		V_b V_c	0 1	V_c V_b	$d_{\gamma\beta}$	0 0 1 0 1 0
		V_b V_c	1 1	V_b V_b	$d_{\gamma\alpha}$	0 1 0 0 1 0

Table 2.3 shows the duty cycles and the corresponding switching states of the matrix converter in case that the rectifier sector 1 is active. The switch output commands for the proposed remedial technique are assigned exactly the same as the output commands for the normal mode control. As a result, the proposed algorithm does not need modification of the existing control hardware.

2.4 Simulation results

To illustrate the feasibility of the proposed PWM modulation strategy for fault-tolerant operation, the modulation technique was simulated with a matrix converter operating with the switching frequency and the output frequency of 5 kHz and 75 Hz, respectively. Figure 2.11 shows the output waveforms at the normal mode operation. The output currents generated by the normal mode control form a three-phase balanced sinusoidal set with 120° phase-shift with respect to each other. The transformed currents in the $\alpha\beta$ axis have sinusoidal waveforms with 90° phase angle.

The proposed matrix converter operation in the fault mode is illustrated in Fig. 2.12, in case of *C*-phase open condition. The output current in *C*-phase, I_C is zero. The output currents in the two remaining healthy phases, I_A and I_B, are regulated with a sinusoidal form with 60° phase displacement with respect to each other. From the point of view of the control strategy, the $\alpha\beta$ current components, expressed in the stationary reference frame, do not have to be affected by the opened phase fault, since the transformed α-β currents are related to torque and flux [18]. Therefore, the $\alpha\beta$ currents transformed from the two remaining healthy phase currents after the *C*-phase open fault still produce sinusoidal waveforms with 90° phase angle, as the normal mode operation [18].

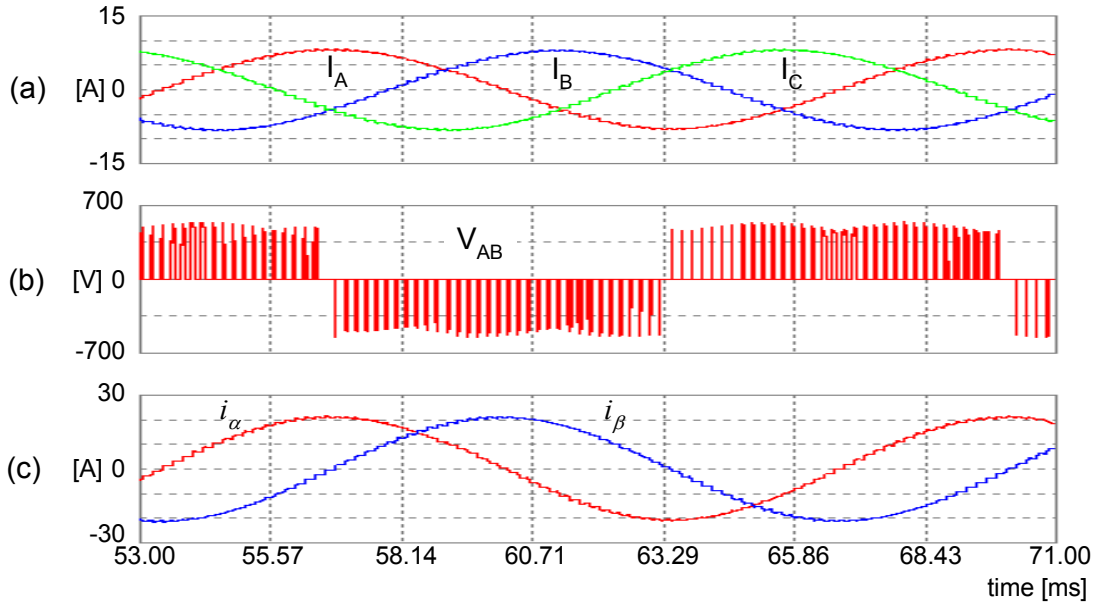


Fig. 2.11 Waveforms in normal mode

(a) output currents (b) output line-to-line voltage (c) transformed $\alpha\beta$ currents.

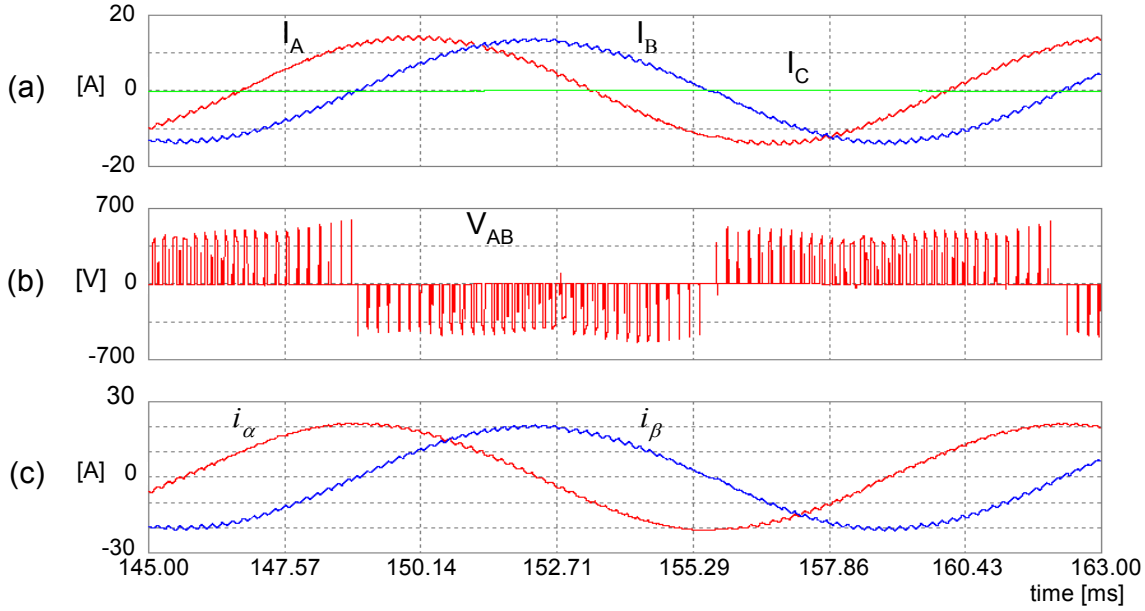


Fig. 2.12 Waveforms in fault mode with opened phase *C*

(a) output currents (b) output line-to-line voltage (c) transformed $\alpha\beta$ currents.

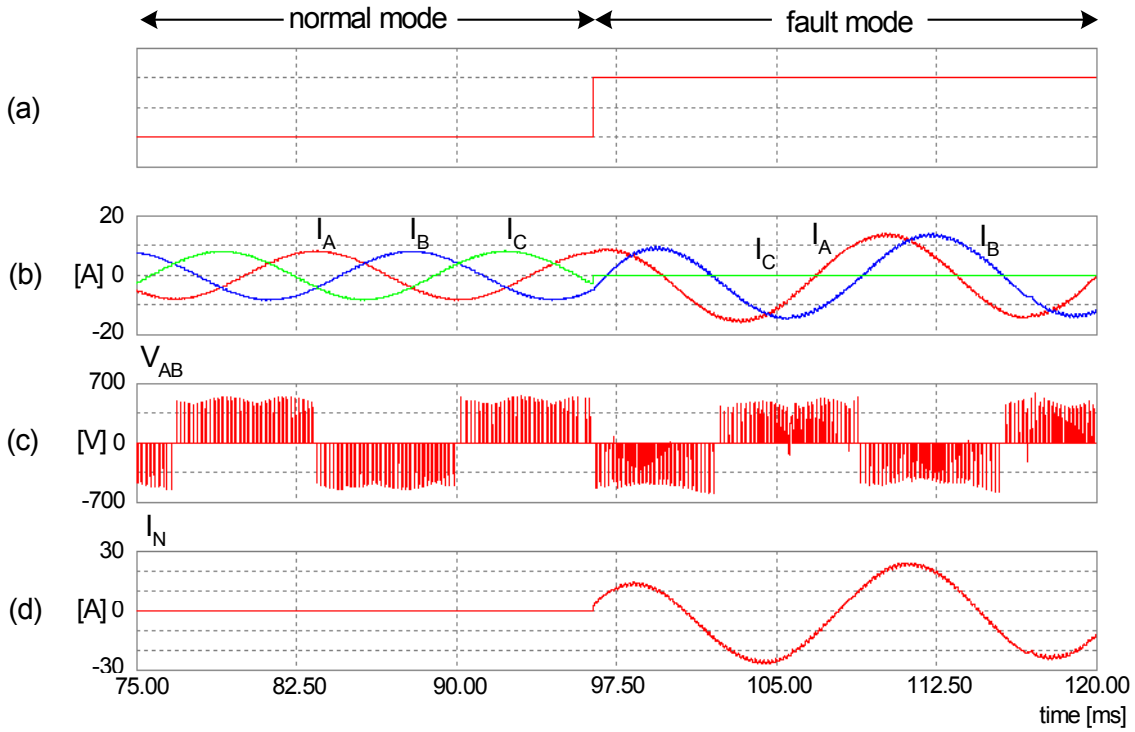


Fig. 2.13 Transient waveforms during open-phase loss on *C*-phase (a) fault signal (b) output currents (c) output line-to-line voltage (d) neutral current.

Figure 2.13 shows the transient operation of the matrix converter from the normal to the fault mode of the *C*-phase loss. With the fault mode signal of the opened *C* phase, the *C*-phase is promptly disconnected from the overall circuit, and the motor neutral is connected to the supply neutral by firing the connecting device. Consequently the output current I_C drops to zero. The proposed PWM strategy for the fault mode is initiated to control two remaining phase currents I_A and I_B, with magnitude increased by a factor of $\sqrt{3}$ and 60° phase-shift with respect to each other. The neutral current equal to the sum of I_A and I_B, begins to flow with the neutral connection due to the asymmetrical two-phase structure.

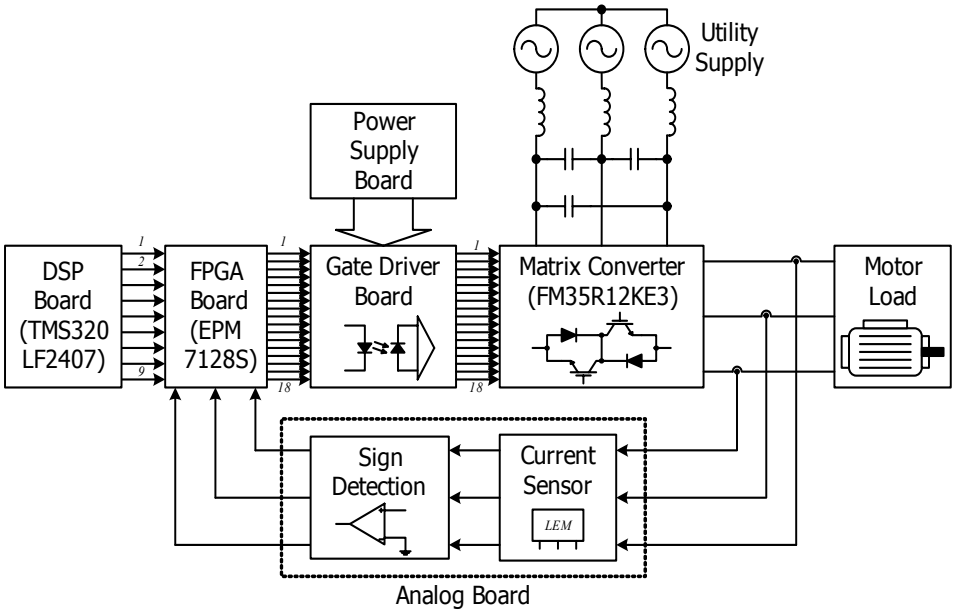
2.5 Experimental results

To validate the proposed control algorithm for the fault-tolerant matrix converter, the prototype of the matrix converter was developed in the laboratory. Figure 2.14 illustrates a functional block diagram and a laboratory prototype of the matrix converter setup. The setup is composed of a digital signal processor (DSP) board (TMS320LF2407), a field-programmable gate array (FPGA) board (Altera EPM7128S), six isolated power supplies, gate drives, an analog board containing current sensors and sign detection circuits for the four-step commutation, and a matrix converter module (Eupec FM35R12KE3) with 18 insulated gate bipolar transistors (IGBTs). The control algorithms for the normal and the fault mode operation have been realized in the DSP board. The complete gate signal commands of the matrix converter are generated by the DSP board with the aid of the FPGA board for the safe commutation.

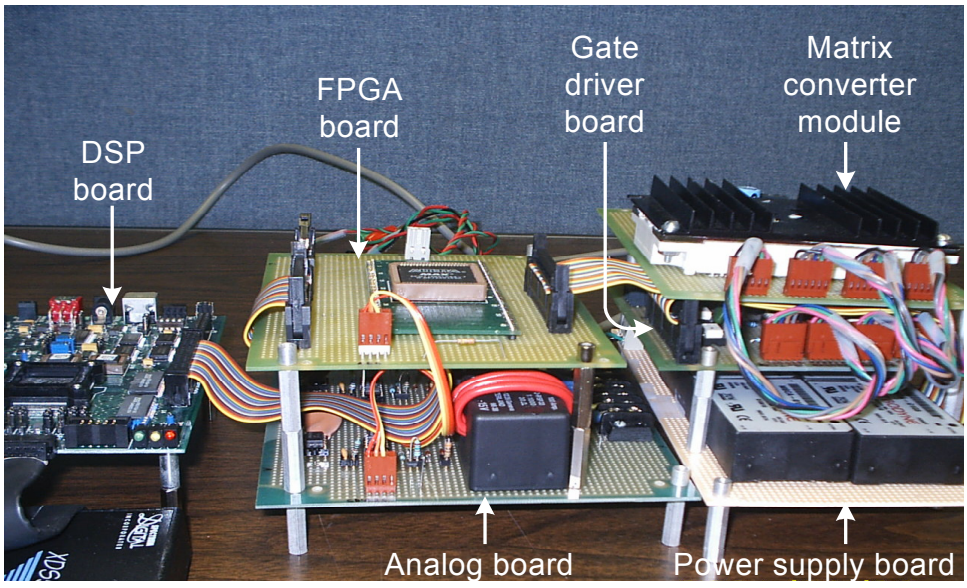
Figure 2.15 illustrates the experimental results of the output currents and voltage measured on the matrix converter prototype working in the normal mode. In the experiment, the matrix converter was operated with 3 kHz switching frequency and 45 Hz output frequency. The sinusoidal output currents are regulated with 120° phase shift with respect to each other. Two output phase currents and voltage controlled by the proposed fault-tolerant operation are shown in Fig. 2.16. It is seen that the two healthy phase currents are controlled with sinusoidal shape with 60° phase displacement with respect to each other.

Figure 2.17 depicts the steady-state current waveforms of the two remaining output phases after opened phase fault. In addition, the transient response is also shown from the normal mode to the fault mode in which the output phase *C* is open-circuited. During the test, the fault occurrence on the *C*-phase was emulated by forcing the active state of a digital input. After the fault, which occurs with the fault detection signal, the output phase *C* is open-circuited by disabling the gate commands of the *C*-phase switches. Thus, the current I_C drops to zero. The two remaining currents on the phase A

and B, I_A and I_B become sinusoidal with the increased magnitude and 60° phase displacement by the fault tolerant control.

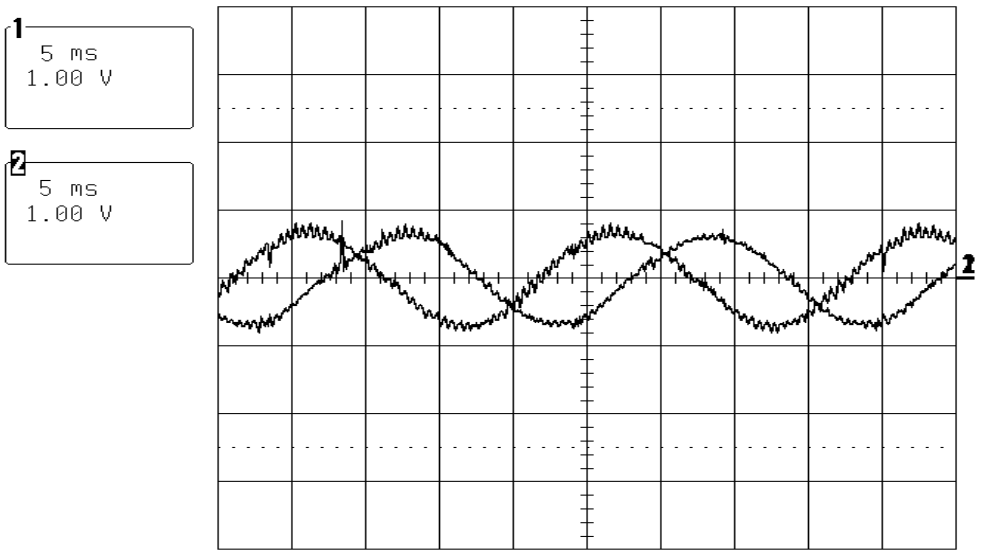


(a)

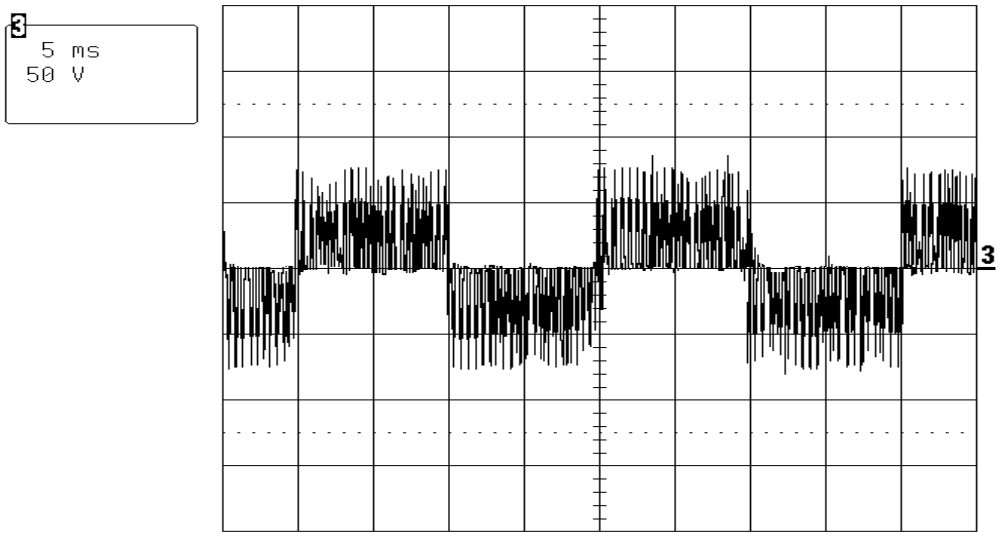


(b)

Fig. 2.14 Experimental setup (a) functional block diagram (b) laboratory prototype.

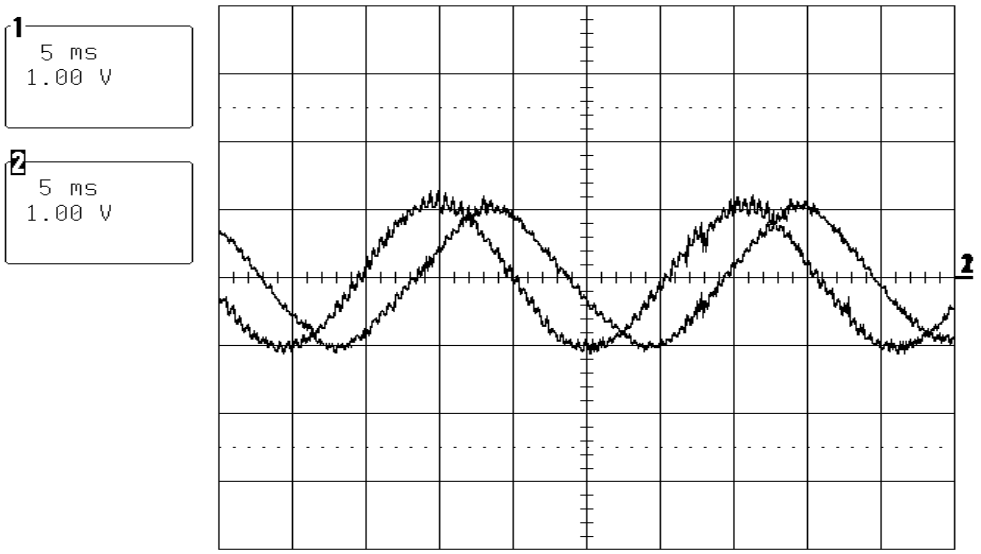


(a)

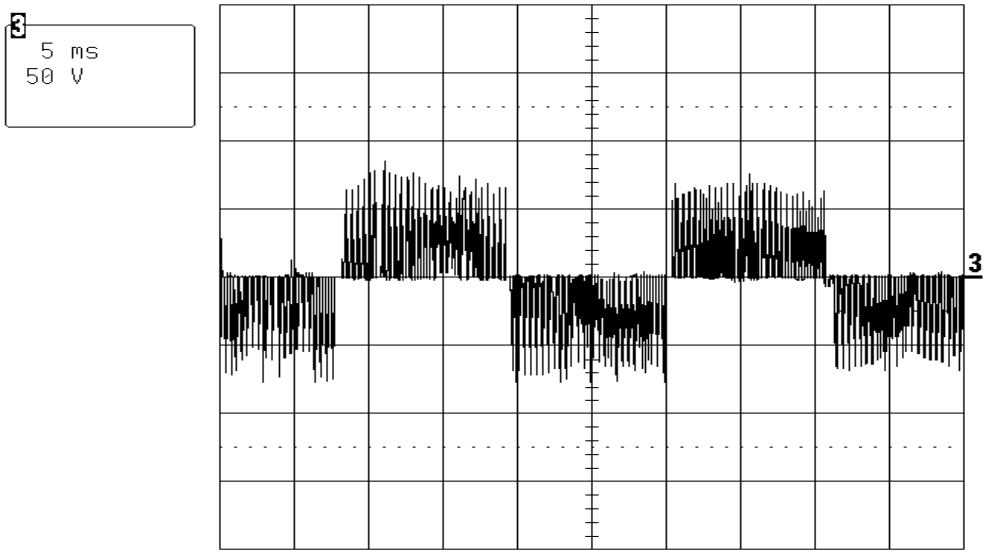


(b)

Fig. 2.15 Normal mode operation (a) output currents (1A/div, 5ms/div) (b) output voltage (50V/div, 5ms/div).

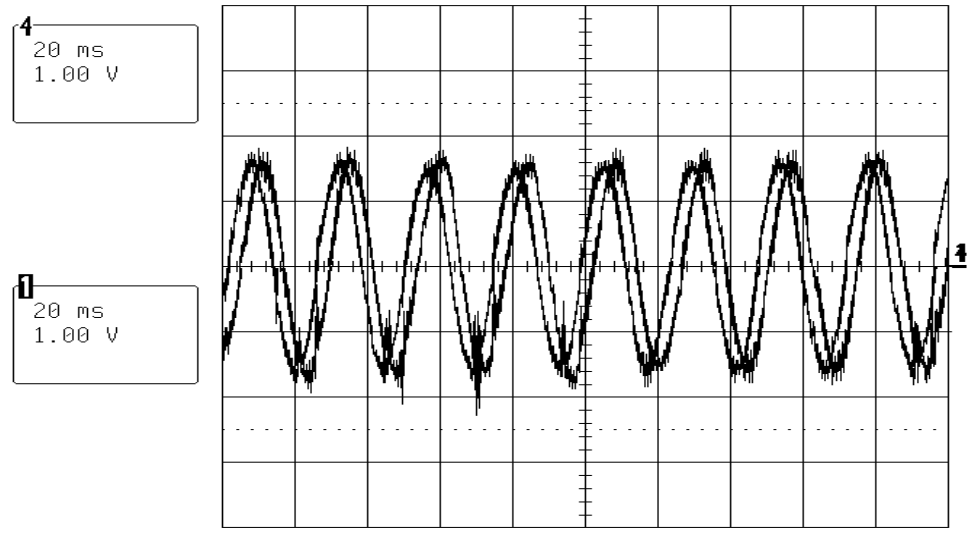


(a)

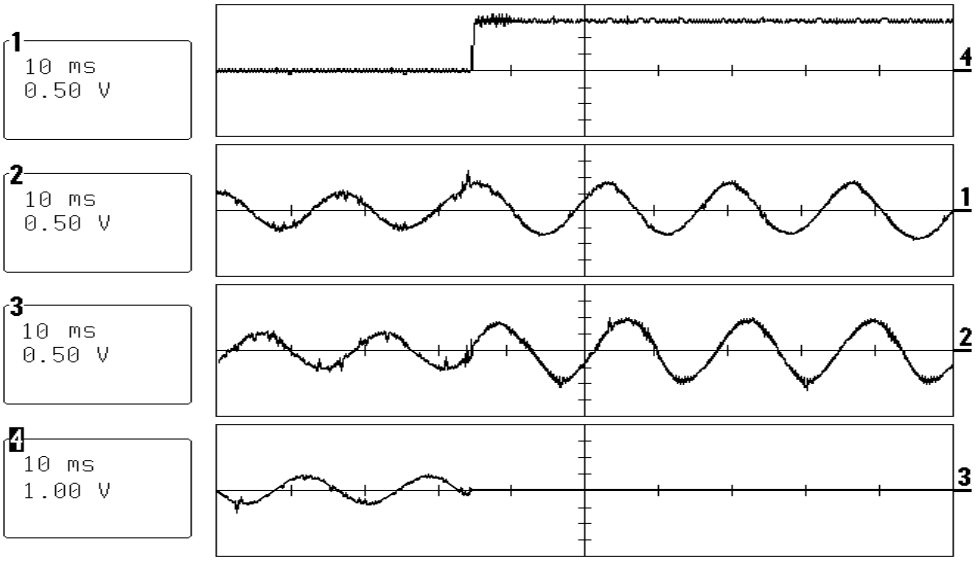


(b)

Fig. 2.16 Fault mode operation (a) output currents (1A/div, 5ms/div) (b) output voltage (50V/div, 5ms/div).



(a)



(b)

Fig. 2.17 Waveforms (a) steady-state current waveforms in the fault mode (b) transient waveforms during the fault occurrence on phase *C* (trace 1: phase *A* current, I_A (0.5A/div), trace 2: phase *B* current, I_B (0.5A/div), trace 3: phase *C* current, I_C (0.5A/div), trace 4: fault detection signal (0: normal mode, 1: fault mode)).

2.6 Conclusion

This chapter proposes a PWM modulation strategy for fault-tolerant operation of the matrix converter drives against opened phase fault. After one of the matrix converter legs is lost, the proposed modulation control makes it possible to keep continuous operation by regulating the two remaining currents shifted by 60° with respect to each other. The modulation technique is developed based on the equivalent model with the fictitious dc-link. Because the post-fault structure leads to an asymmetric two-phase drive, it is necessary to construct two virtual dc-link voltages in the fictitious dc-link by the rectifier stage control. Two-phase operation is obtained through the inverter stage control based on the two imaginary dc-link voltages. The proposed fault compensation strategy is achieved with no hardware modification in the converter structure and no redundant backup legs. Thus, the proposed fault control can improve system reliability of the matrix converter drives with minimal cost increase associated with the motor neutral connection. It should be noted that the input currents are not sinusoidal during the fault mode operation due to the asymmetric two-phase operation. Since the fault operation means an emergency operating condition, the input current quality is assumed to be a secondary concern. Furthermore, the use of the matrix converter drives under fault is usually intended to operate for short time period necessary for the maintenance schedule. Simulation and experimental results have been shown to verify the proposed modulation method for improving the reliability of three-phase matrix converter drives.

CHAPTER III

HYBRID AND HIGH-PERFORMANCE CONVERTER BASED ON LOAD COMMUTATED INVERTER AND VOLTAGE SOURCE INVERTER*

3.1 Introduction

This chapter proposes a hybrid, high-performance ac/ac power converter using a parallel assembly of a load commutated inverter (LCI) and a voltage source inverter (VSI) for high power applications. As explained in the section 1.3.2.1, the drawbacks by the capacitor commutation and the dc-commutation circuit offset the advantages of the LCI topology suitable for high-power areas. In addition, the six-step output current waveforms and intrinsic slow dynamics of the LCI are far from high performance.

In the proposed hybrid converter, the high-power LCI provides real power to loads, whereas the medium-power VSI conveys reactive and harmonic power to loads. Thanks to the combined operation of two inverters, sinusoidal output currents/voltages are obtained. The VSI allows fast dynamic response for the hybrid structure. In addition, the proposed hybrid converter utilizes the VSI to make a leading power factor for the LCI natural commutation. By avoiding the use of the large output capacitors and the dc-commutation circuits for the LCI commutation, this converter can eliminate all problems caused by them in the conventional LCI topologies. Therefore, the developed compound converter enhances the LCI topology with high performance as well as solution of the commutation problems by capacitors and dc-commutation circuits. Note that target areas for the proposed hybrid converter are high-power applications, where single standalone

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PWM-VSI cannot be applied to generate sinusoidal output quantities because of its limited power capability.

This hybrid converter has the following features and advantages.

1. The leading power factor required for load commutation of the LCI is fully provided by the VSI in all operating regions. This safe commutation for the LCI is produced by active control of the leading angle through the VSI, rather than the passive capacitor commutation.
2. All problems caused by the output capacitors in the conventional LCIs, such as fundamental and harmonic resonance, and inherent instability in the high frequency region, can be solved since the VSI emulates the output capacitors.
3. By avoiding the use of complex and costly forced dc-commutation circuit, the potential risk of commutation failure regarding the dc-commutation circuit and the torque pulsation of motor loads can be eliminated.
4. Both load currents and voltages are nearly pure sinusoidal, containing little harmonic components.
5. The proposed converter shows fast dynamic response by the VSI operation.
6. Minimum VSI rating and cost are achieved by the proposed strategy.

The operational principles, control, and features such as losses of the proposed converter are investigated and described in detail. Simulation and experimental results are shown to support the feasibility of the proposed topology and control structure.

3.2 Proposed hybrid converter

3.2.1 Topology and properties

A complete power circuit diagram of the proposed system is illustrated in Fig. 3.1. It is composed of a three-phase controlled rectifier, a load commutated inverter

followed by a dc-link inductor, and a three-phase voltage source inverter [37]. The voltage source inverter is connected with the load commutated inverter in parallel through a small LC filter. The VSI can be supplied from an isolated diode rectifier followed by a dc-link capacitor, or a dc battery as a dc source. Note that although this configuration is similar to the topology of an active power filter or a tandem inverter, its purpose and operation are quite different from them [31]. An inductive load is represented by an induction motor.

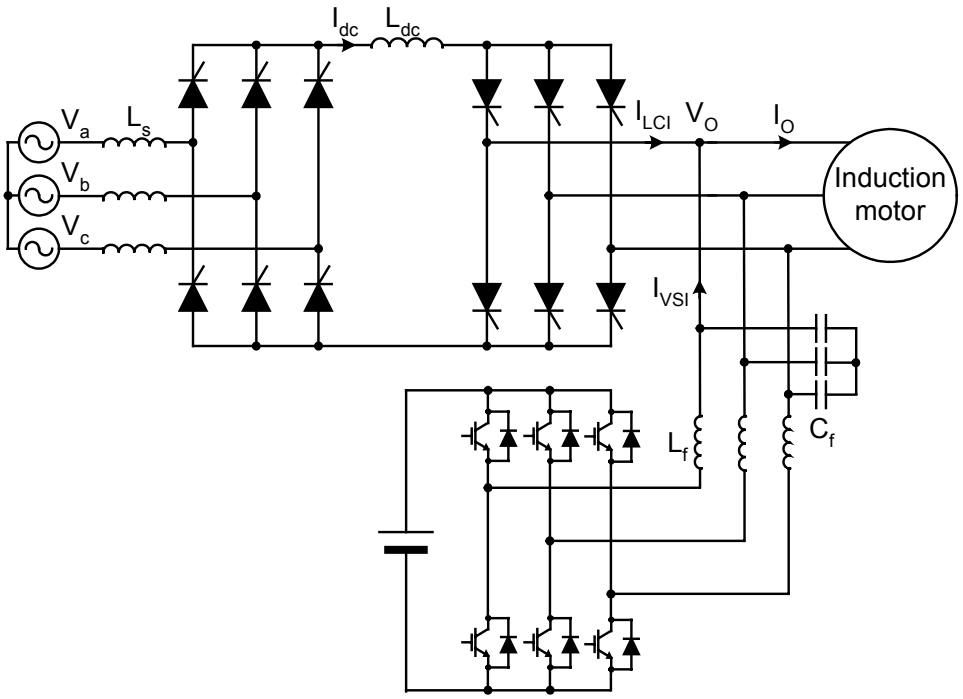


Fig. 3.1 Circuit diagram of proposed system.

The LCI operates in the quasi-square-wave mode with converter-grade thyristors. Consequently, thyristors in the LCI naturally turn on and off only once per cycle of the output current and therefore, their switching loss is negligible.

The main function of the VSI is to apply sinusoidal phase voltages to the motor load in order to regulate the motor speed as well as provide a safe commutation angle for the LCI. The motor speed is controlled by transiently adjusting the output voltage

amplitude and frequency of the VSI. In addition, the phase angle of the output voltage is achieved by shifting the firing angle of the LCI suitably to obtain a safe load commutation angle. Therefore, the leading power factor for the LCI operation is entirely obtained by the VSI over the whole speed range of the induction motor. Based on the leading power factor for the LCI provided by the VSI, the proposed system can run an induction motor without the dc-commutation circuit as well as output ac capacitors of the conventional LCI based induction motor drives. As a result, the proposed system can successfully solve all problems caused by the output capacitors and the forced dc-commutation circuit. In addition, the proposed scheme can generate sinusoidal output voltages and currents for all operating regions, leading to a reduction in the low-order harmonics injected into the motor load. This allows elimination of the torque pulsation and harmonic losses due to motor currents with quasi-square-wave of the conventional LCI. A small LC filter is required to smooth out the pulsewidth-modulated voltages generated by the VSI.

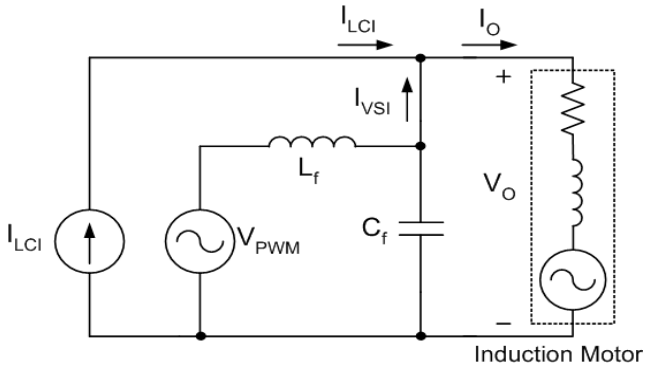


Fig. 3.2 Per-phase equivalent circuit of proposed system.

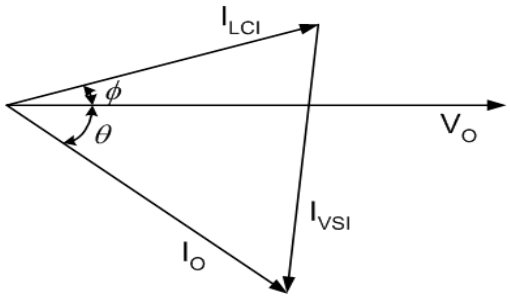


Fig. 3.3 Vector diagram of proposed system.

Figure 3.2 shows a per-phase equivalent circuit of the proposed system. The proposed system has a parallel connection of two inverters, the LCI represented by the current source I_{LCI} and the VSI represented by the voltage source V_{PWM}. The VSI impresses a sinusoidal output voltage V_O to the motor. Moreover, it controls leading power factor for safe commutation of the LCI. The output current I_O is determined by the sinusoidal output voltage V_O controlled by the VSI. Concurrently, the LCI also supplies a current I_{LCI} to the motor load. Therefore, the output current I_O is the sum of the LCI output current, I_{LCI} and the VSI output current, I_{VSI}. From the operating point of view, the fast VSI operates as a master inverter and the slow LCI as a slave. As a result, the proposed system can show a fast system transient response compared with the conventional LCI-based topologies since the proposed system has time response close to the sampling period of the VSI.

Figure 3.3 shows a current vector diagram of the proposed system. The phase angle ϕ represents the leading power factor angle for safe commutation of the LCI. This angle is controlled by adjusting the phase angle between the output voltage and the gating instant of the LCI. Therefore, this strategy ensures safe commutation of the LCI over all operating speeds of the induction motor. The phase angle θ denotes the power factor angle of the induction motor. In terms of power rating supplied to the motor load, the LCI supplies the real power to the load, while the VSI provides the small real power corresponding to phase shift between the LCI output current and the output voltage, as well as the reactive and the harmonic power. The LCI is not comparable to the VSI from cost point of view. Therefore, the VSI power rating should be kept to a minimum to make the proposed system a cost-effective solution. Because the VSI should supply its output current equal to the difference between the motor current, I_O and the LCI output current, I_{LCI}, the VSI output current, I_{VSI} is proportional to the phase angle between I_{LCI} and I_O, corresponding to $\phi + \theta$. Thus, the phase angle $\phi + \theta$ should be maintained at a minimum value for small VSI rating. This condition can be obtained by adjusting the leading angle ϕ to the minimum value satisfying safe commutation, and controlling the induction motor power factor. Since a high-power induction motor has better power

factor characteristics than a small rating motor, it is expected that the power factor angle θ is small in high power applications. It makes the proposed system more competitive and useful for high power areas.

3.2.2 Control system structure

The general control block diagram of the proposed hybrid converter for the purpose of induction motor drives is shown in Fig. 3.4. The overall control strategy is composed of two main control loops.

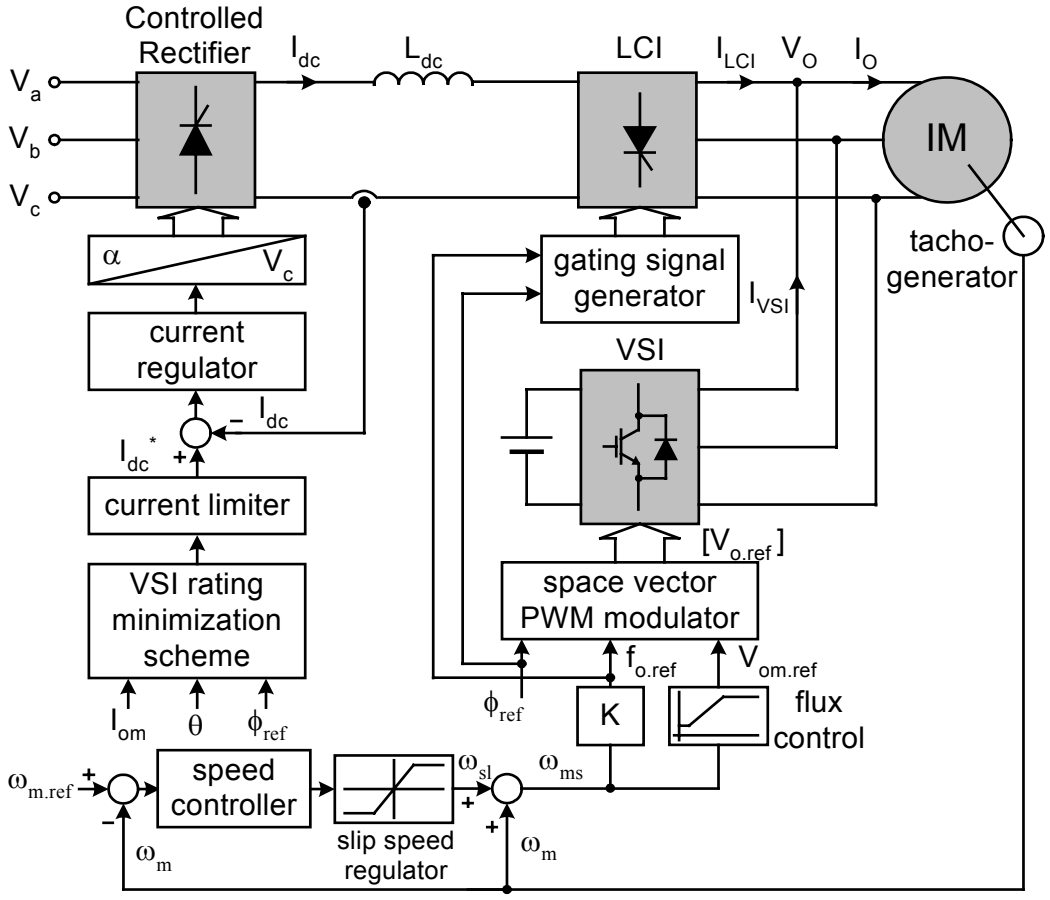


Fig. 3.4 Overall control scheme of proposed hybrid converter.

The first control loop is the motor speed control based on operation of the VSI. The motor speed can be regulated using closed loop speed controller using the slip speed regulator, which determines the slip speed reference. The synchronous speed, obtained by adding the actual speed and the slip speed, sets the inverter operating frequency. The voltage amplitude command then is set from the inverter frequency using a function generator, which ensures a nearly constant flux operation. Finally, the phase angle of the motor voltage is decided in order to provide a leading power factor (ϕ) for the safe commutation of the LCI. The space-vector modulator produces the switching pattern based on the amplitude, frequency, and phase command signal for the sinusoidal output voltage of the VSI. This speed loop control implemented by the VSI ensures a fast dynamic response with much faster sampling period than the conventional LCI.

The second control loop is for the dc-link current control using the controlled rectifier. This scheme varies the dc-link current in order to keep the VSI rating minimized at steady state. The main function of this loop is to set the dc-link current reference in such a way that the VSI rating is minimized, based on the motor current amplitude and the phase angle $\phi + \theta$. The next section theoretically demonstrates that the converter rating of the VSI can be effectively minimized by properly adjusting the dc-link current.

3.2.3 VSI rating minimization strategy

Since the proposed hybrid converter consists of two inverters, the output power distribution between them, given a certain output power requirement, is important. A rating factor η is defined as the ratio of the LCI rating and the VSI rating. Note that two inverters are connected with the same motor phase voltage in their output terminals by assuming that voltage drop due to the output LC filter for the VSI is negligible. Therefore, the rating factor is directly proportional to the ratio of rms values of the VSI output current and the LCI output current as

$$\eta = \frac{S_{VSI}}{S_{LCI}} = \frac{I_{VSI.rms}}{I_{LCI.rms}} \tag{3.1}$$

Large VSI required for the drive results in a very high system cost, which will limit the proposed system. From cost point of view, the LCI is not comparable to the VSI. As a result, it is desirable to minimize the rating factor under an operating power required for the induction motor load. In order to derive the dc-link current control to minimize the VSI rating, the dc-link stage of the LCI is modeled by an ideal ripple-free current source. Figure 3.5 illustrates the plots of output currents of the two inverters, the motor phase voltage, and the motor current. Since the motor currents are sinusoidal quantities and the LCI currents have no ripple components in the dc-link, the LCI output current and the motor current are expressed by

$$I_{LCI}(\omega t) = \frac{2\sqrt{3}I_{dc}}{\pi}\left(\cos\omega t - \frac{1}{5}\cos 5\omega t + \frac{1}{7}\cos 7\omega t \cdots\right)$$

$$I_O(\omega t) = I_{om}\cos(\omega t + (\phi + \theta)) \tag{3.2}$$

where, I_{om} is the amplitude of the sinusoidal motor phase current. The rating factor can be derived, using (3.1) and (3.2), by

$$\eta = \sqrt{1 - \frac{3I_{om}}{I_{dc}}\left\{\frac{\sqrt{3}}{\pi}\cos(\phi + \theta) - \frac{I_{om}}{4I_{dc}}\right\}} \tag{3.3}$$

In (3.3), it should be noted that motor phase current amplitude I_{om} depends on the motor shaft speed and leading power factor angle ϕ is a control factor for the safe commutation of the LCI. In addition, θ is the lagging power factor angle of the induction motor, which is detectable. Then, the dc-link current value, which minimizes the VSI rating, can be obtained by setting the derivative of η with respect to the dc-link current to zero,

$$\frac{d\eta}{dI_{dc}} = 0 \tag{3.4}$$

This yields an dc-link current command I_{dc}^{*} given by

$$I_{dc}^{*} = \frac{I_{om}}{\left(2\sqrt{3}/\pi\right)\cos(\phi + \theta)} \tag{3.5}$$

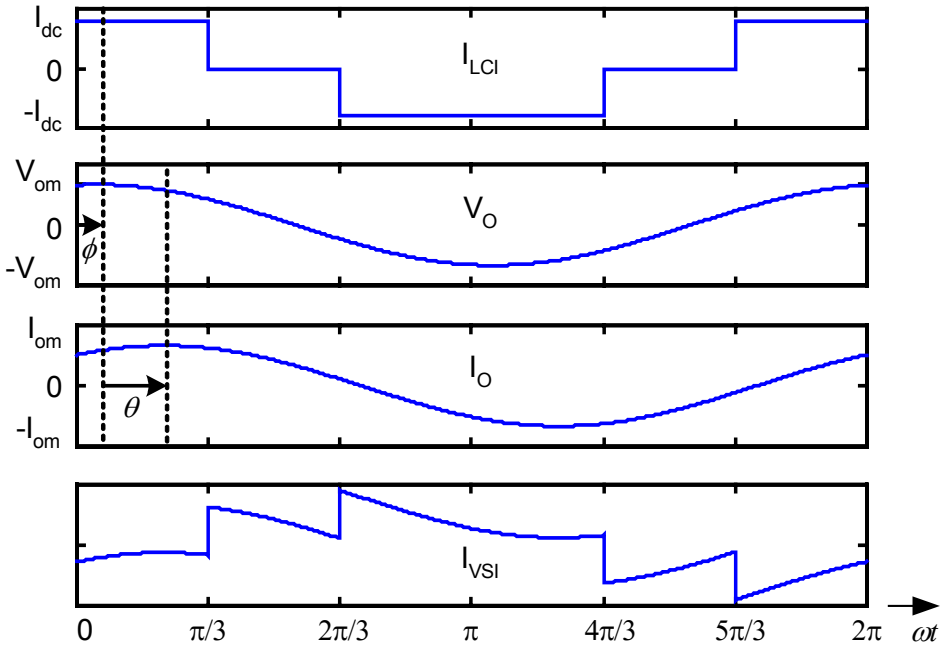


Fig. 3.5 LCI output current, motor phase voltage, motor current, and VSI output current.

Equation (3.5) allows the dc-link current control to achieve the minimum VSI rating requirement based on the motor current amplitude and phase shift between the motor current and the LCI output current. This dc-link current control algorithm is implemented by the controlled rectifier. It is worth noting that from (3.5), with increased power factor angles $\phi+\theta$, the dc-link current value to minimize the rating factor also increases. Figure 3.6 illustrates the plot of dc-link current command as a function of motor phase current amplitude versus phase angle. The minimized rating factor η_{min} is

$$\eta_{\min} = \frac{3}{\pi}\sqrt{\left(\frac{\pi}{3}\right)^2 - \cos^2(\phi+\theta)} \tag{3.6}$$

It is important to note that the dc-link current value and the corresponding minimized rating factor are unique at every operating point of the induction motor and a given leading power factor angle ϕ. Figure 3.7 shows a minimized rating factor with the dc-link current value of (3.5) as a function of phase angle.

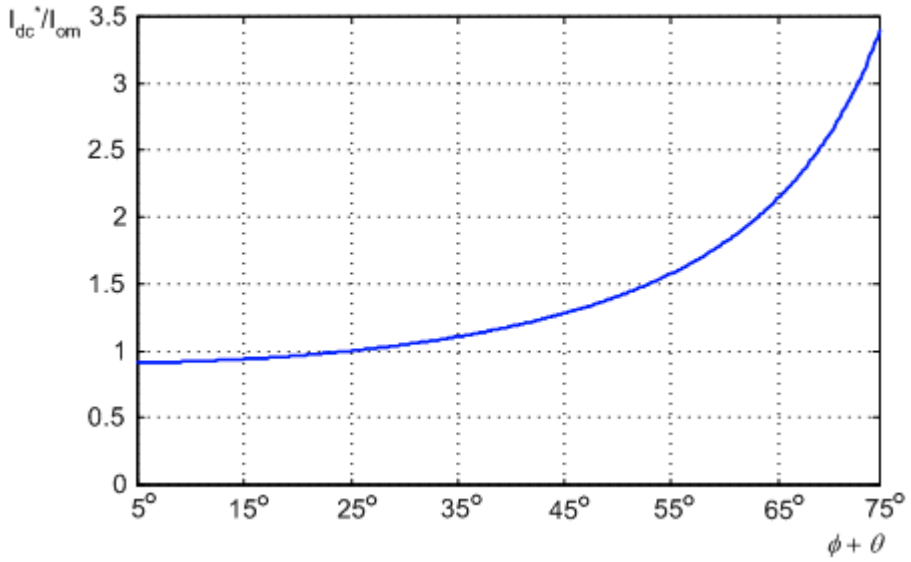


Fig. 3.6 Ratio of dc-link current and motor current amplitude as a function of phase angle.

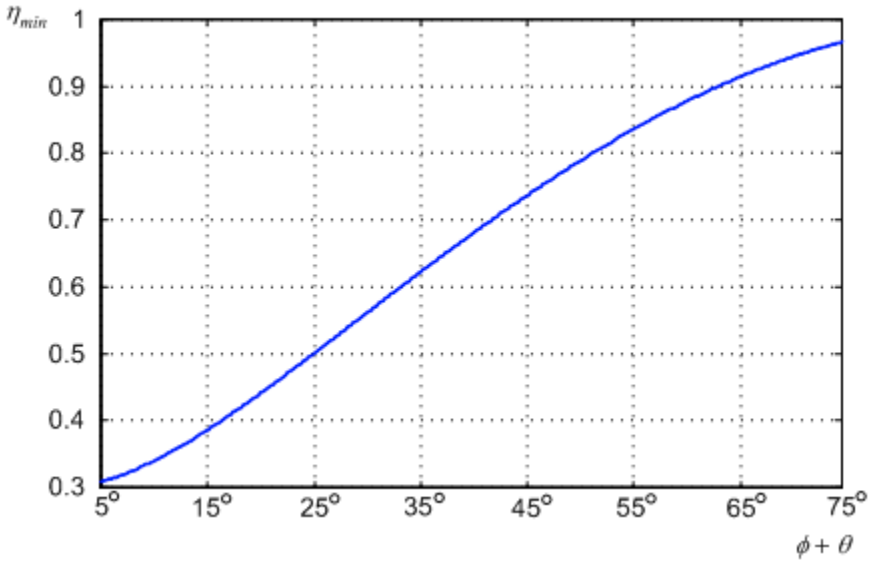


Fig. 3.7 Minimized rating factor versus phase angle.

3.2.4 Loss performances

For high power applications, one important issue is the power semiconductor losses and the efficiency. In the proposed hybrid converter using the LCI and the VSI, the VSI loss performance is of concern because the LCI losses are negligible.

The VSI semiconductor losses in the proposed hybrid converter were determined by simulation based on power converter loss model for different load conditions and switching frequencies [35], [36], [38]. The power losses consist of conduction losses and switching losses. The conduction losses of an IGBT or a diode in the VSI can be modeled using the on-state voltage drop and the conducting current by the VSI. The on-state voltage drops were obtained from the manufacturer's data sheet by applying a first-order curve fitting of the on-state loss characteristics, depending on the conducting currents obtained in the simulation model [35]. The data were chosen from EUPEC N-Channel IGBT BSM100GB120DLCK with 1200V and 100A rating. The conduction losses of the IGBT and the diode were abbreviated to P_{condT} and P_{condD}, respectively. The switching losses were, similarly, decided by measuring the switching energy as a function of the conduction current and then modeling it by a first-order relationship. The turn-on and turn-off switching energy characteristics were also found from the data sheet, according to the conduction current. Constant junction temperature of T_j=125°C was used for the loss performance calculation. Acronyms of P_{offD}, P_{offT}, and P_{onT} denote the diode turn-off losses, the IGBT turn-off losses, and the IGBT turn-on losses, respectively. To assess the VSI losses in the hybrid converter, the power losses in a standalone VSI were also simulated and compared, because the proposed hybrid converter is comparable to the standalone VSI to generate sinusoidal motor currents from the standpoint of motor load terminals. The distinct difference between two VSIs is the power components to be delivered. The real power is supplied by the standalone VSI, whereas the VSI in the proposed hybrid converter delivers the harmonic power and reactive power. Figure 3.8 depicts the VSI losses for various motor displacement power

factor θ. The standalone VSI and the VSI in the proposed hybrid structure are denoted by *VSI(s)* and *VSI(h)*, respectively. It is shown that the VSI losses of the proposed hybrid

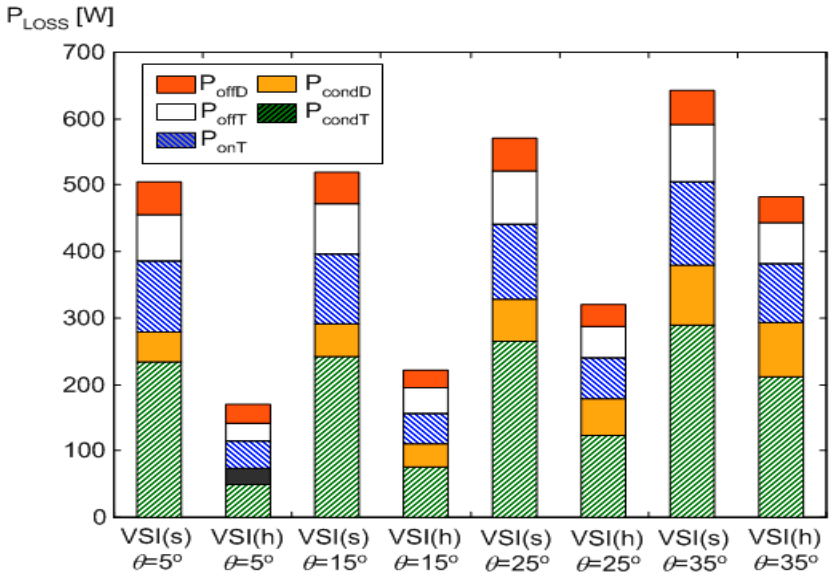


Fig. 3.8 VSI losses at different motor displacement angles (φ=5°, f_s=5kHz, f_o=60Hz, V_{dc}=1200V, m_{inv}(V_{om}/V_{dc})=0.85, P_o=100kW, T_j=125°C).

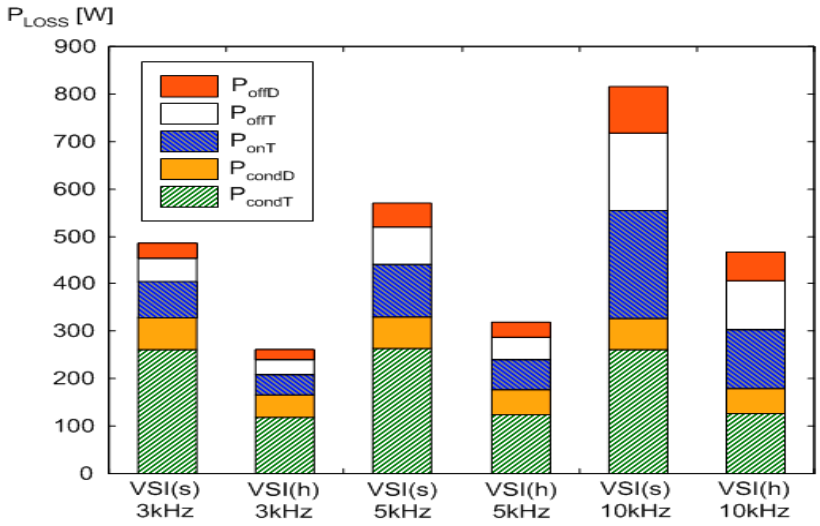


Fig. 3.9 VSI losses at different switching frequencies (φ=5°, θ=25°, f_o=60Hz, V_{dc}=1200V, m_{inv}(V_{om}/V_{dc})=0.85, P_o=100kW, T_j=125°C).

system, *VSI(h)* are reduced by more than 50% of the standalone VSI losses for θ less than 25°. However, the difference of the two VSI losses is reduced with the increasing θ angles of the induction motor. As a result, it is important to control the induction motor with good power factor, as pointed out before. The losses of the two VSIs are illustrated with different switching frequencies in Fig. 3.9. The VSI losses in the proposed hybrid converter are reduced by half of the standalone VSI losses, regardless of the switching frequencies.

3.3 Simulation results

In order to investigate the performance of the proposed hybrid converter, a detailed computer simulation was performed using a 500 hp induction motor whose parameters are given as

Rated power : 500 hp	Inertia(J) : 11.06 [kgm^2]
Number of poles : 4	
R_s : 0.262 [Ω]	X_{ls} : 1.206 [Ω]
R_r : 0.187 [Ω]	X_{lr} : 1.206 [Ω]
X_M : 54.02 [Ω]	

Figure 3.10 depicts the motor shaft speed under full load. Motor shaft speed was set to 900 rpm, resulting in the frequency of inverter being 30 Hz. Figure 3.11 shows the three-phase motor phase currents and the LCI output currents at steady-state. The motor phase current has a phase delay with respect to the LCI output current, corresponding to the sum of leading power factor angle (ϕ) and load power factor angle (θ). The leading power factor angle (ϕ) is controlled for the safe commutation of thyristors using the VSI. A 10° leading angle (ϕ) between the motor phase voltages and the gating instants of the LCI was used to ensure safe commutation for corresponding thyristor switches. On the other hand, the load power factor angle (θ) between the motor phase voltage and the

motor phase current is determined by the motor characteristics, which was about 30° in this simulation. The dc-link current command I_{dc}^{*} was set by (3.5) in order to minimize the VSI rating. It is noticed that the dc-link current I_{dc} is regulated to about 18% higher value than the motor current amplitude I_{om} with 40° phase shift angle between the LCI and the motor currents. Figure 3.12 shows the LCI output current, the motor phase current, the VSI output current, and the dc-link inductor current at steady state, respectively. It can be noted that the VSI output current provides the difference between the motor phase current and the LCI output current in order to supply the active power for the phase shift as well as the reactive and harmonic power to the motor. The dc-link inductor current shows some harmonic ripple components because of the finite dc-link inductor, which appear in the LCI output current.

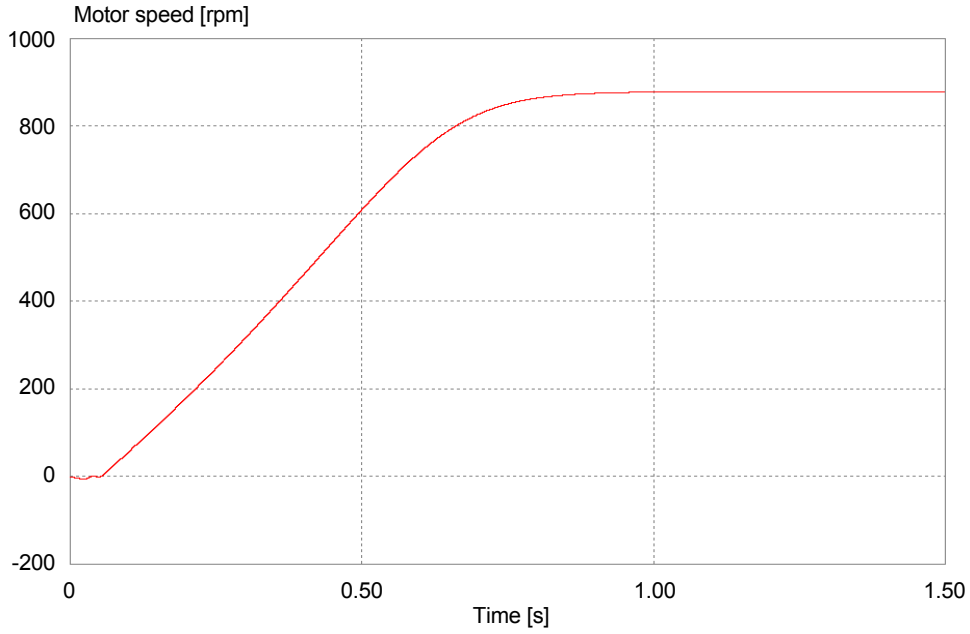


Fig. 3.10 Induction motor shaft speed under full load.

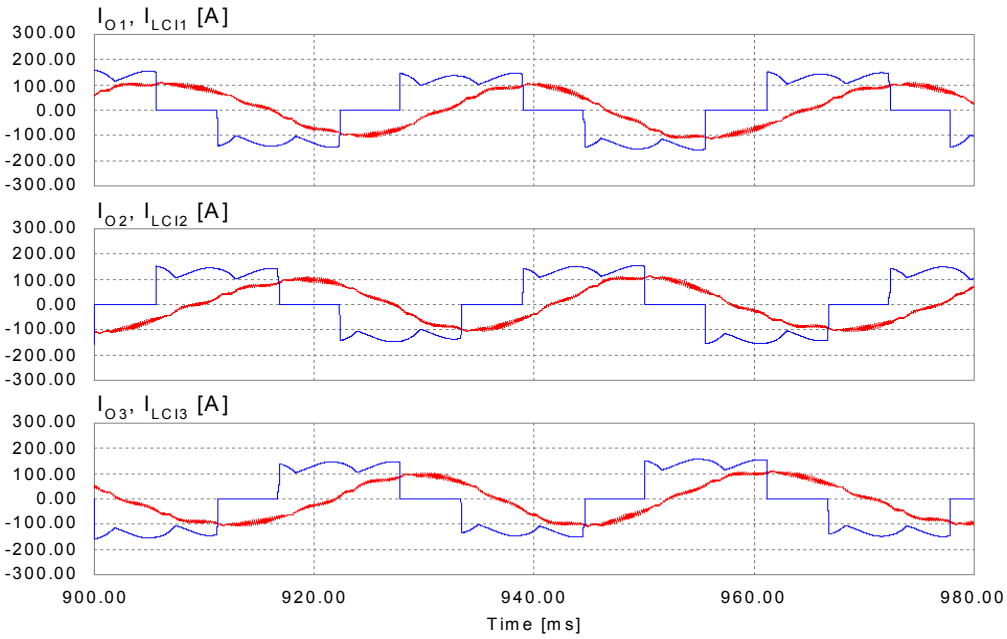


Fig. 3.11 Motor currents and LCI output currents at steady state.

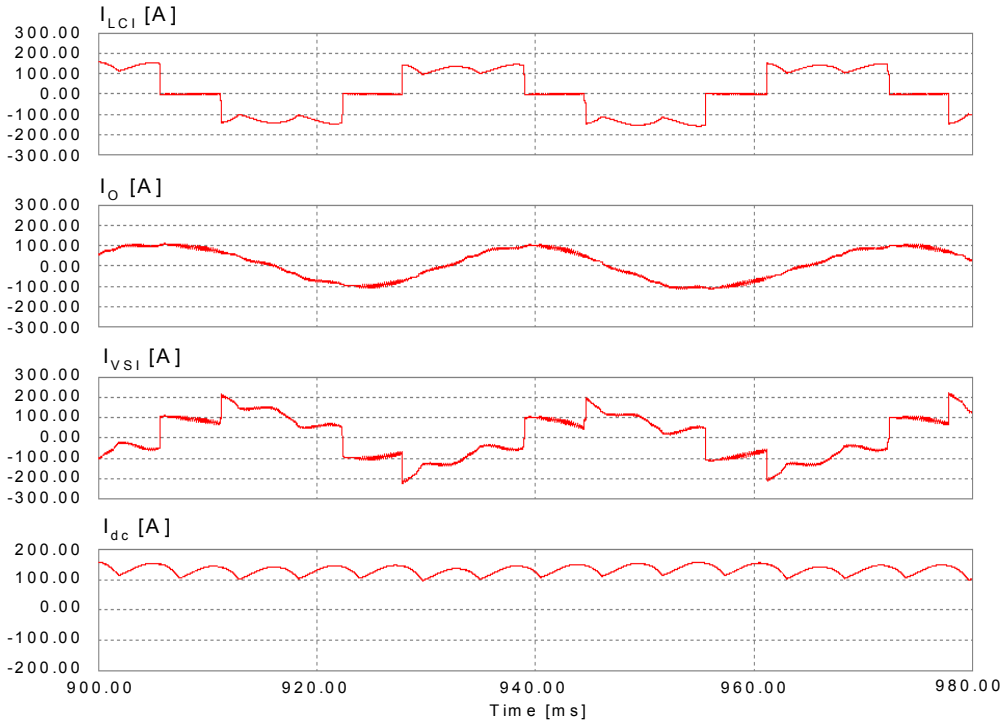
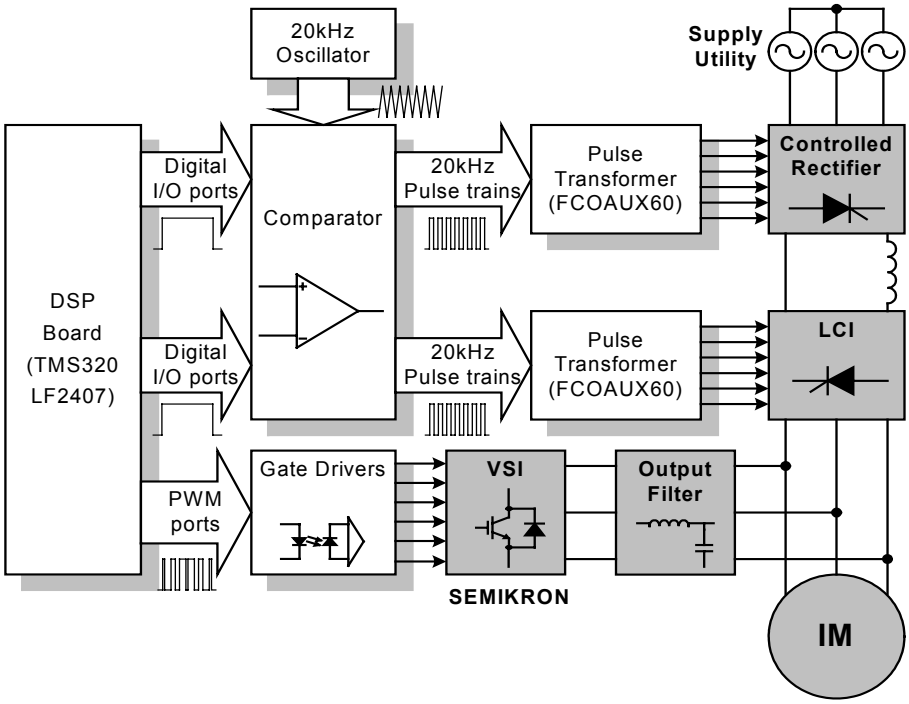


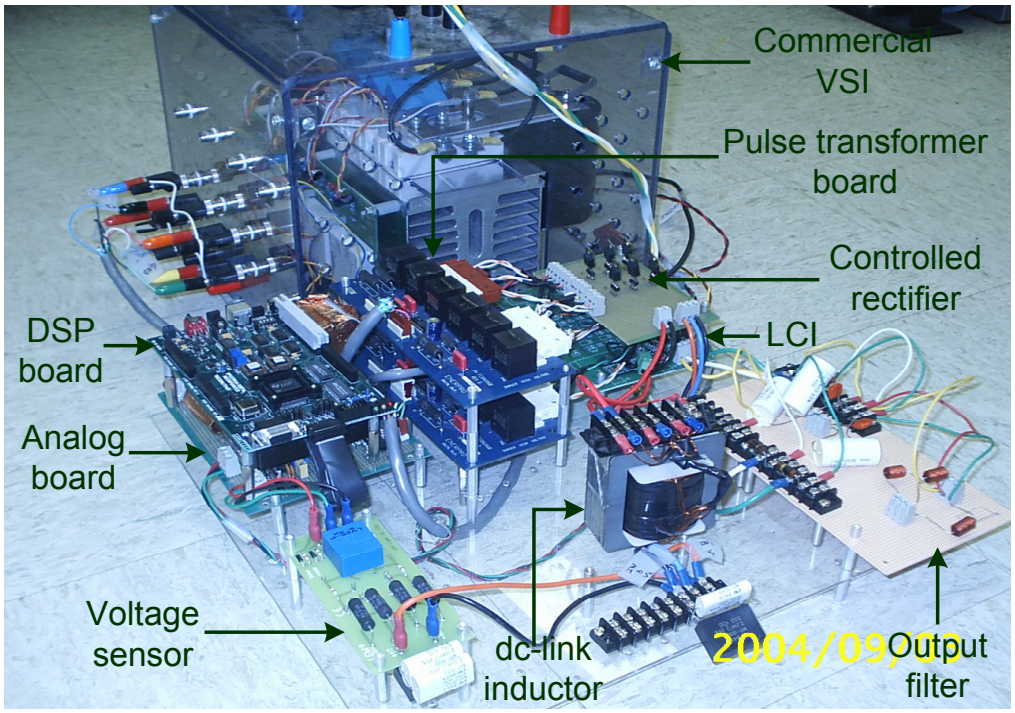
Fig. 3.12 LCI output current, motor current, VSI output current, and dc-link inductor current.

3.4 Experimental results

To validate the proposed hybrid topology and control algorithm, the prototype hybrid converter was developed using a LCI, a phase-controlled rectifier, and a VSI. An IGBT-based commercial inverter (SEMIKRON) was employed as the VSI. In addition, prototypes of a phase-controlled rectifier and a LCI were fabricated in the laboratory. A 120mH dc-link inductor was used for the LCI. The proposed control structure was implemented with a fixed-point digital signal processor (DSP) board (TMS320LF2407). The VSI control signals were provided through PWM ports of the DSP board. On the other hand, the gate pulse commands of the controlled rectifier and the LCI were generated with digital I/O port signals of the DSP board and 20kHz external oscillator signal due to limited PWM ports of the DSP board. The pulse trains through pulse transformer boards (FCOAUX60) were used to turn on the thyristors of the controlled rectifier and the LCI. In the experiment, a 230V, 60Hz, 1 hp general-purpose induction motor was employed as the load. A three-phase output filter was implemented with a 0.5mH inductor and a 50μF capacitor. The block diagram and the photo of the setup are shown in Fig. 3.13.



(a)



(b)

Fig. 3.13 Experimental setup (a) functional block diagram (b) laboratory prototype.

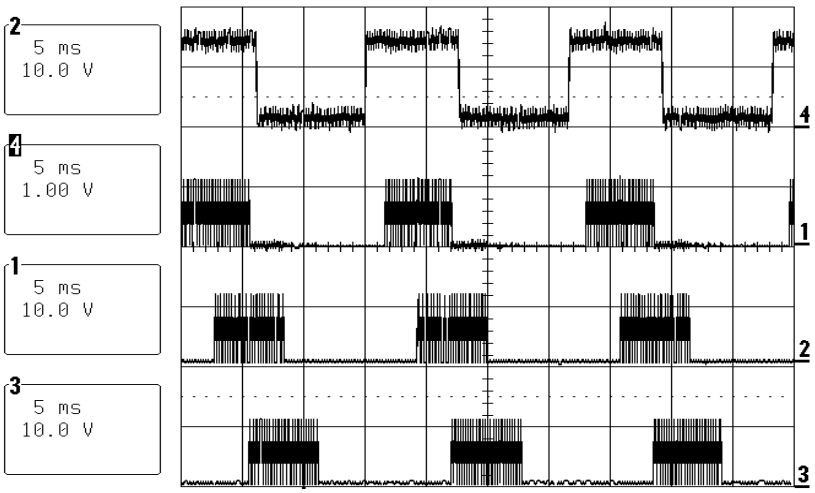
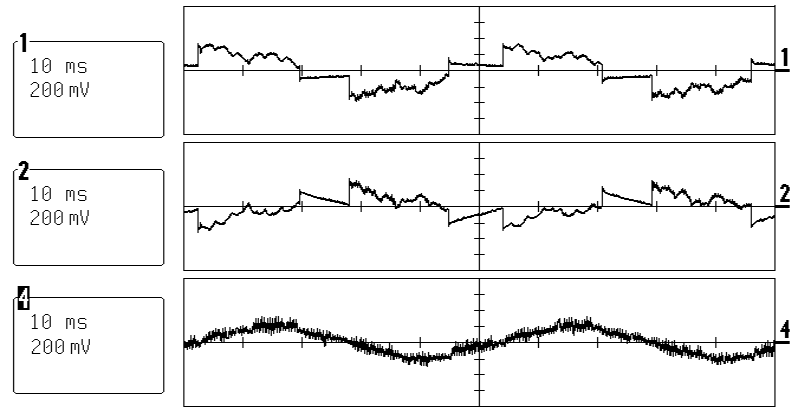


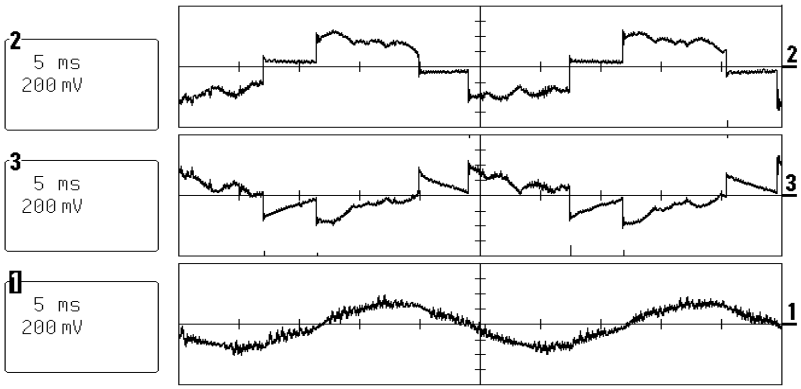
Fig. 3.14 ZCD signal and gating signals of controlled rectifier.

Figure 3.14 shows the gating pulses for the controlled rectifier along with the output of the zero crossing detector (ZCD) for the supply voltage. The pulse train has 20 kHz frequency and 50% duty cycle to avoid the saturation of the pulse transformer. The ZCD signal from the supply voltage is used to determine the firing instants for the controlled rectifier. Steady-state operation of the proposed system with different output frequency (20 Hz, 40 Hz, and 60 Hz) is illustrated in Fig. 3.15. The current waveforms show that the motor currents are sinusoidal with little harmonics and the VSI injects output currents corresponding to the difference between the LCI and the motor current.

Figure 3.16 illustrates the LCI output current and the motor phase voltage. A leading power factor angle (ϕ) between the LCI output current and the motor phase voltage was set to 5° to ensure safe load commutation. Based on this angle, the LCI can operate successfully without any commutation failures over all speed ranges. Figure 3.17 shows the LCI output current and the motor current at steady state. Since the 40° phase angle (ϕ+θ) between the LCI and the motor current was detected, the dc-link current I_{dc} was regulated to about 18% higher value than the motor current amplitude by the proposed control strategy to minimize the VSI power rating.



(a)



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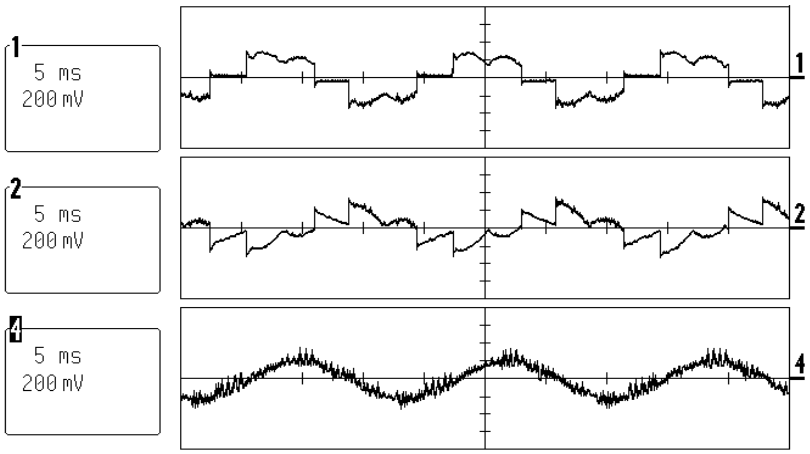


(c)

Fig. 3.15 Output current waveforms at steady state (a) at 20 Hz (b) 40 Hz (c) 60 Hz (upper trace: LCI output current (1A/div), middle trace: VSI output current (1A/div), lower trace: motor current (1A/div)).

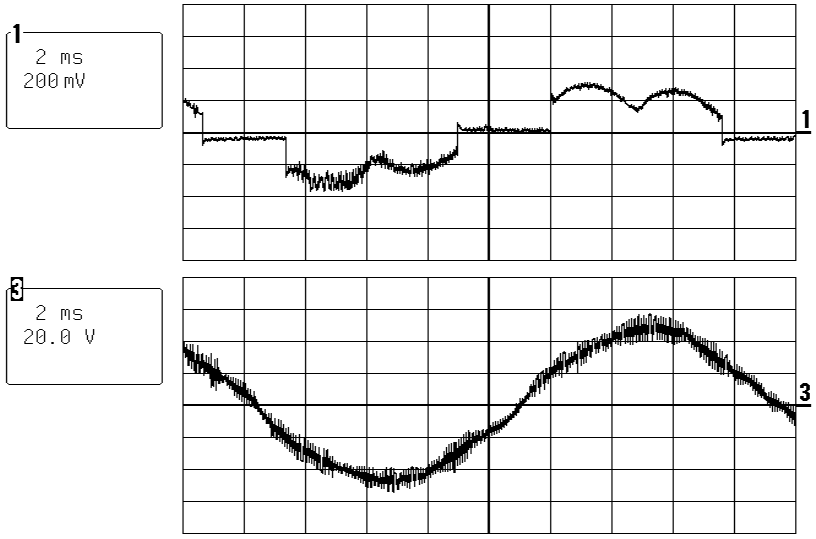


Fig. 3.16 LCI output current and motor phase voltage
(1A/div and output frequency of 60 Hz).

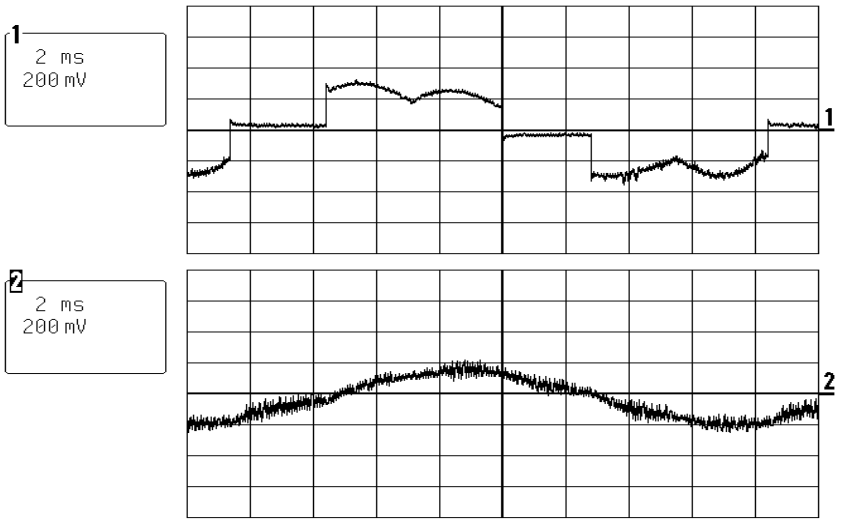
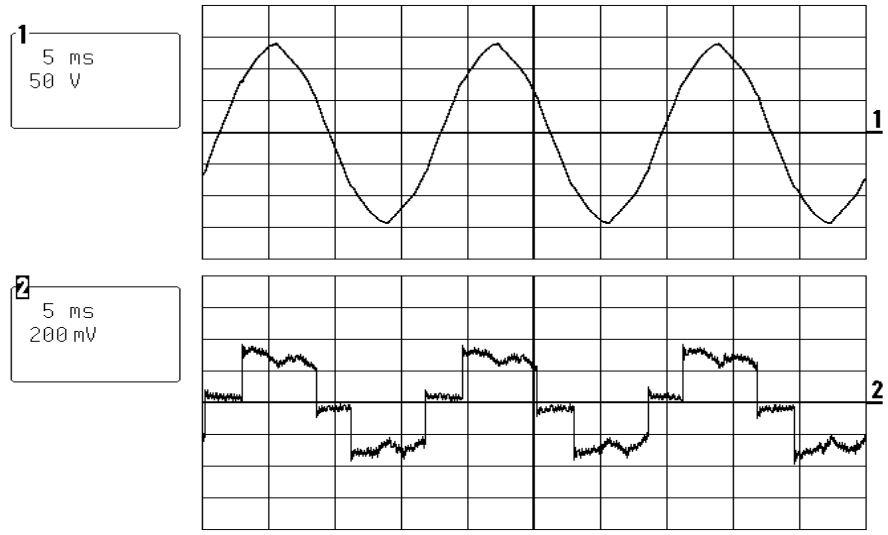


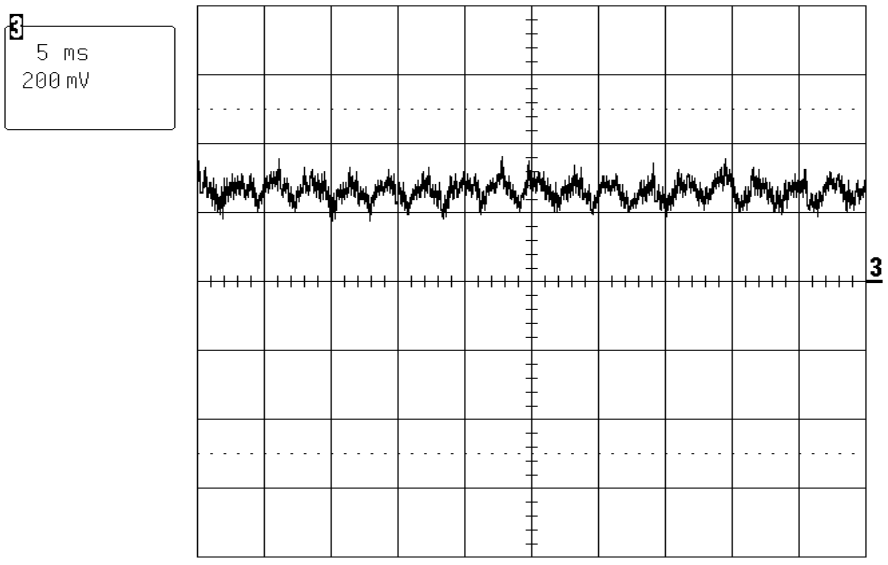
Fig. 3.17 LCI output current and motor current
(1A/div and output frequency of 60 Hz).

Figure 3.18 shows the supply line voltage, the input current of the controlled rectifier, and the dc-link current. The dc-link current is regulated by the phase shift information between the LCI output current and the motor current. Figures 3.19 and 3.20

depict the output current waveforms under a rapid amplitude change and a rapid frequency change, respectively.



(a)



(b)

Fig. 3.18 (a) Supply voltage (50V/div) and controlled rectifier input current (1A/div) (b) dc-link current (1A/div).

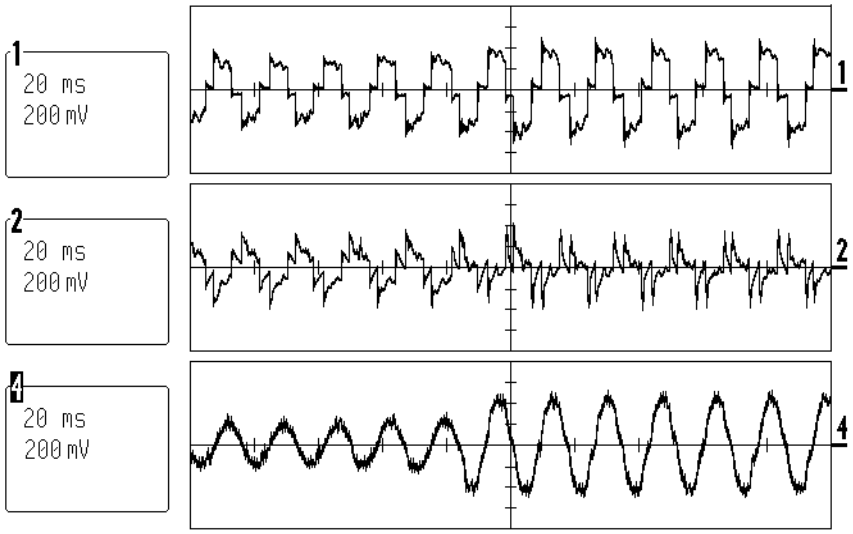


Fig. 3.19 Output current waveforms with a rapid amplitude change at 60 Hz output frequency (upper trace: LCI output current (1A/div), middle trace: VSI output current (1A/div), lower trace: motor current (1A/div)).

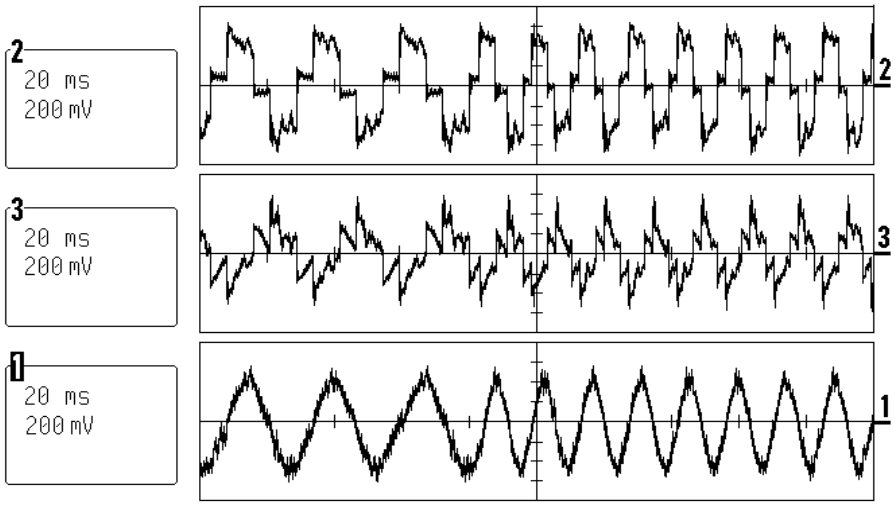


Fig. 3.20 Output current waveforms with a frequency change from 30 Hz to 60 Hz (upper trace: LCI output current (1A/div), middle trace: VSI output current (1A/div), lower trace: motor current (1A/div)).

3.5 Alternative scheme

3.5.1 Topology and features

The hybrid converter in Fig. 3.1 employs the controlled rectifier and the uncontrolled rectifier to control the LCI and the VSI, respectively. However, both the LCI and the VSI can be fed from single diode rectifier by introducing a dc-dc buck converter, as shown in Fig. 3.21 [38]. The buck converter is brought between the diode rectifier and the LCI, in order to convert uncontrolled dc voltage to controlled dc current. The dc-link current regulated by the buck converter is supplied to the LCI.

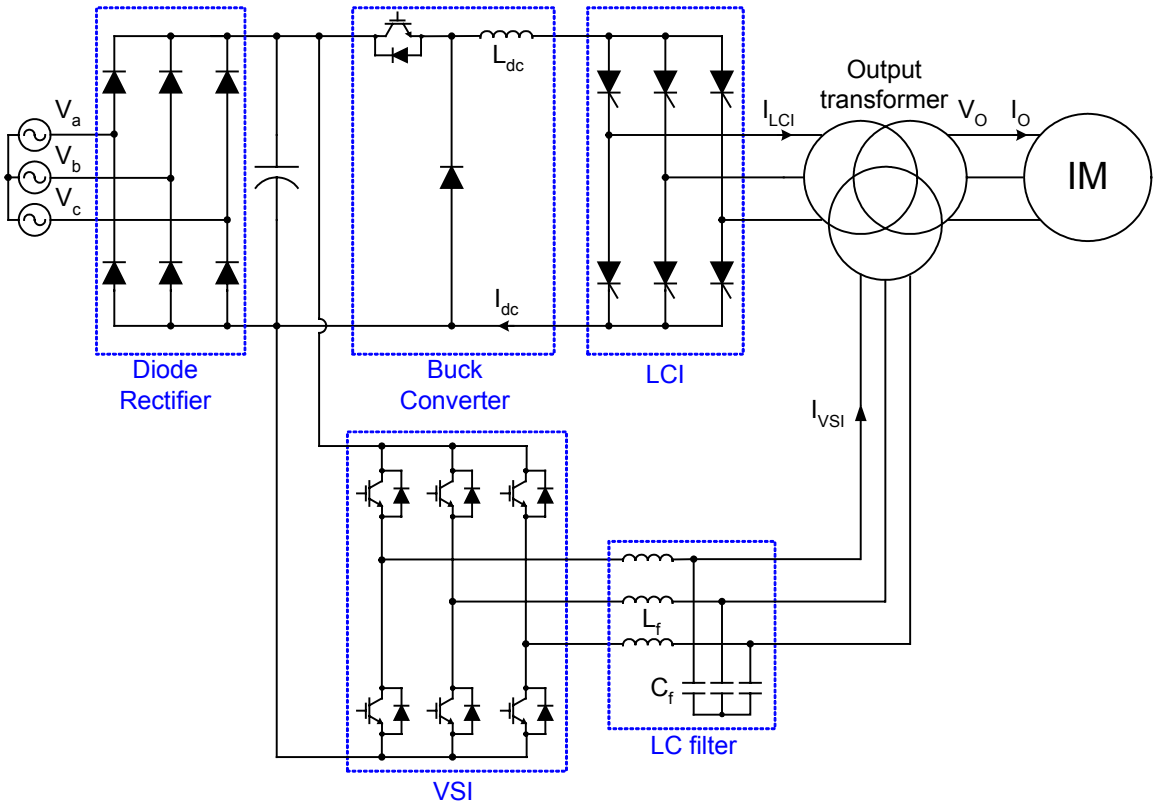


Fig. 3.21 Alternative topology of hybrid converter system.

Distinct advantage by bringing the buck converter is greatly reduced dc-link inductor size, along with elimination of the controlled rectifier. The dc-link current control performed by the controlled rectifier in Fig. 3.1 is now achieved through the buck converter. The output transformer is selected to provide isolation between the LCI and the VSI, as well as output voltage step-up/down.

3.5.2 Simulation and experimental results

Simulation results in Fig. 3.22 show the output current waveforms of the hybrid converter with the buck converter. In the simulation, the dc-link inductance was set to 5mH. The switching frequencies for the VSI and the buck converter were 3 kHz and 300 Hz, respectively. As before, the sinusoidal motor current is obtained with a phase delay with respect to the LCI output current, which corresponds to the sum of leading angle (ϕ) and the load angle (θ). Note that the only difference is the flat waveform of the LCI output current.

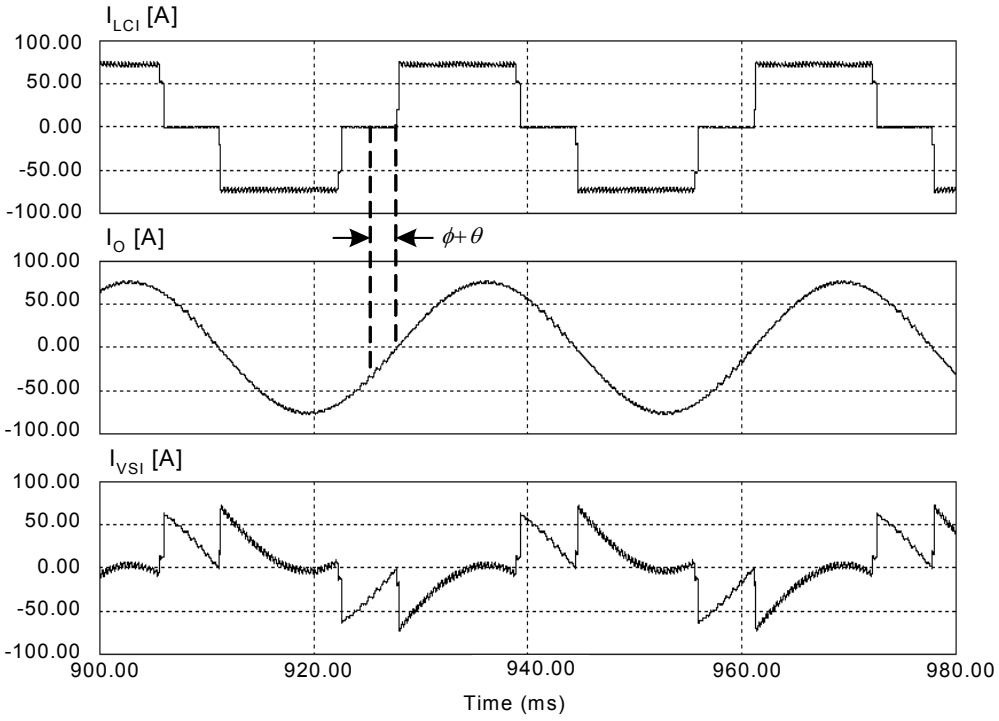


Fig. 3.22 LCI output current, motor current, and VSI output current.

The experimental current waveforms with a 35 Hz output frequency are also illustrated in Fig. 3.23. A 3mH dc-link inductor and a 230V, 60 Hz, 1 hp general-purpose induction motor were used for the experiment. A three-phase output filter was implemented using a 0.5mH inductor and a 50μF capacitor. Figure 3.24 shows the dc-link current controlled by the buck converter. It is illustrated that the accurate current regulation of the dc-link current is achieved with a small dc-link inductor.

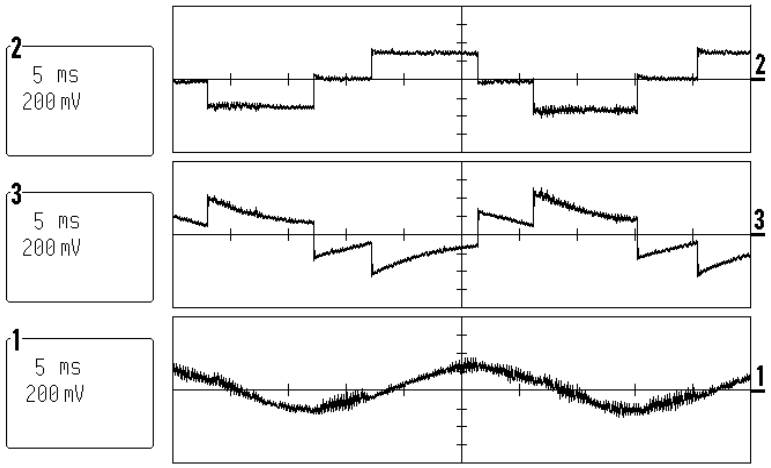


Fig. 3.23 Output current waveforms at steady state at 35Hz (upper trace: LCI output current (1A/div, 5ms/div), middle trace: VSI output current (1A/div, 5ms/div), lower trace: motor current (1A/div, 5ms/div)).

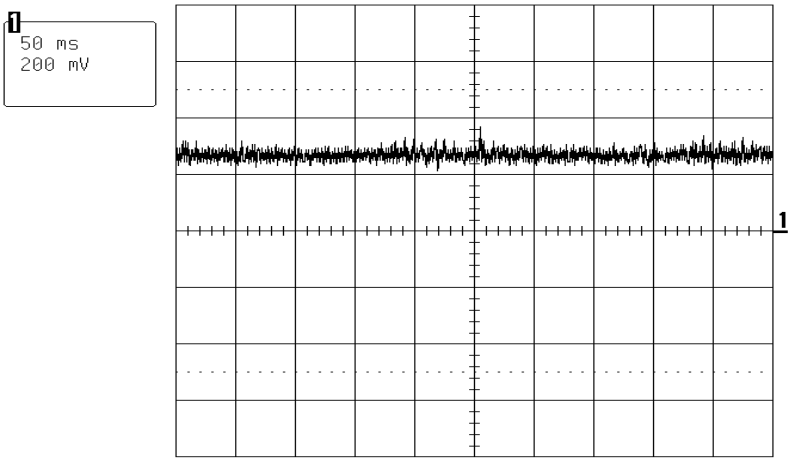


Fig. 3.24 DC-link current (1A/div, 50ms/div).

Figure 3.25 illustrates the LCI output current and the motor phase voltage. The LCI output current and the motor current at steady state are shown in Fig. 3.26

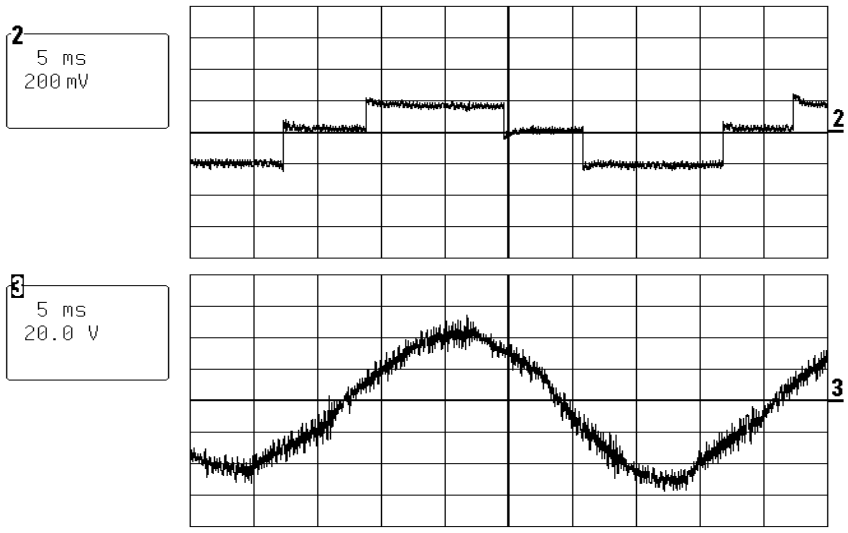


Fig. 3.25 LCI output current (2A/div, 5ms/div) and
motor phase voltage (20V/div, 5ms/div) at 35Hz.

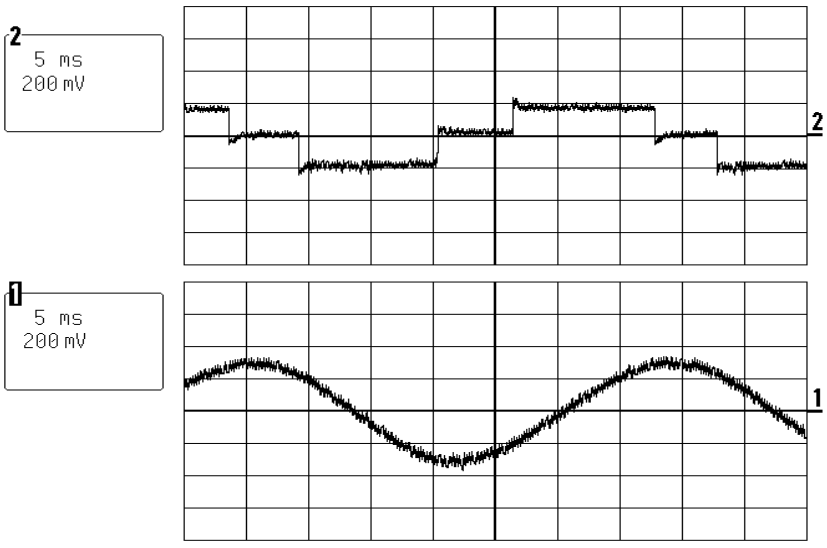


Fig. 3.26 LCI output current (2A/div, 5ms/div) and
motor current (1A/div, 5ms/div) at 35Hz.

3.6 Conclusion

In this chapter, a high-power, high-performance hybrid converter is proposed based on the parallel compound of the LCI and the VSI. The proposed strategy allows the operation of the LCI with a safe and active commutation angle provided by the VSI. By eliminating the requirement of the output capacitors and the forced dc-commutation circuit for the conventional LCI topologies, this hybrid converter is quite free from all problems, such as resonance, inherent instability, and torque pulsation of motor loads, caused by the conventional LCI drives. In addition, sinusoidal motor currents/voltages and faster response are obtained by the proposed converter, yielding high performance operation. The dc-link current control strategy has been derived and implemented to achieve minimum VSI power rating according to the phase angle between the motor current and the LCI output current. This chapter shows the simulation and experimental results that validate the feasibility of the proposed topology and control algorithm. Alternative hybrid topology and its results are also included.

CHAPTER IV

CURRENT SOURCE INVERTER WITH ADVANCED FORCED COMMUTATION CIRCUIT AND CONTROL METHOD

4.1 Introduction

This chapter proposes a new six-step current source inverter topology and control with a thyristor-based structure in high-power applications. As mentioned in Chapter I, the conventional autosequentially commutated inverters (ASCIs) have utilized a number of large, high-power ac capacitors and high-power diodes along with complex thyristor-based auxiliary circuits as their forced commutation circuits. The bulky and expensive passive commutation components and complicated control for the auxiliary thyristor circuits have been main causes to fade the ASCIs away, despite of the suitable thyristor-based topologies in high power areas.

Compared to the conventional ASCIs, the proposed current source inverter employs single, small voltage source inverter as a forced commutation circuit. The small VSI, connected in parallel with the large thyristor-based CSI, operates only during commutation instants of load currents, while stops its operation for non-commutation periods. Based on its discontinuous operation for commutation periods, the VSI with low power rating and small size can be utilized in the proposed current source inverter. In the proposed CSI, the VSI operated by proposed control scheme performs three functions as followings:

- Forced commutation of thyristors in the CSI

  By appropriate VSI switching operations, the VSI applies its dc-link voltage to an off-going thyristor with the reverse-biased polarity, resulting in turning off the thyristor.

- Transfer of reactive load energy

  The VSI switching operation enables the reactive load energy of the off-going phase fed back to the on-coming phase during the inductive load commutation. The reactive energy of the off-going phase is temporarily stored in the dc-link capacitor of the VSI, and then transferred to the on-coming phase during the load current commutation.
- Voltage clamping circuit

  The peak voltages across the load terminals and the thyristors are limited to the VSI dc-link voltage level, which can be adjusted by the VSI control.

Therefore, the single VSI completes all tasks required for the commutation process to operate a high-power, six-step CSI. By utilizing the gate-turn-off switches of the VSI, the commutation and the energy transfer process are very simple and safe, resulting in eliminating possible commutation failures. The entire load currents are delivered through the thyristors of the large CSI, whereas the small VSI deals with partial currents during short commutation periods. Thus, the VSI power rating is much smaller than the CSI rating. In recent years, the more and more falling price of the gate-turn-off switching devices with small power rating makes it possible to use a small VSI for the secondary purpose [31]. The proposed CSI can utilize each advantage of the constituent inverters, such as high-power capability of the thyristor-based CSI and easy control of the small VSI with reduced cost.

Simulation and experimental results are shown to demonstrate the feasibility of the proposed CSI structure and control scheme.

4.2 Proposed current source inverter

4.2.1 Topology and description

The topology of the proposed CSI system is illustrated in Fig. 4.1. The proposed system is composed of two different types of inverter configurations, a CSI and a VSI. The CSI is fed through a dc-link inductor and a three-phase controlled rectifier, while the VSI has a dc capacitor as its energy storage element. Note that the circuit structure is similar to the hybrid converter system in chapter III. However, the VSI does not require an independent dc power source obtained by an isolation transformer and a diode rectifier in chapter III.

The large CSI based on thyristors is used as the main inverter to feed and control inductive loads such as induction motors. On the other hand, the small VSI, connected in parallel with the CSI, is employed as an auxiliary inverter. Due to no self-commutation capability of the CSI, the commutation process is performed by the auxiliary VSI. The VSI is designed to operate only during commutation intervals of the load currents, in order to turn off the thyristors in the CSI as well as transfer the reactive load energy.

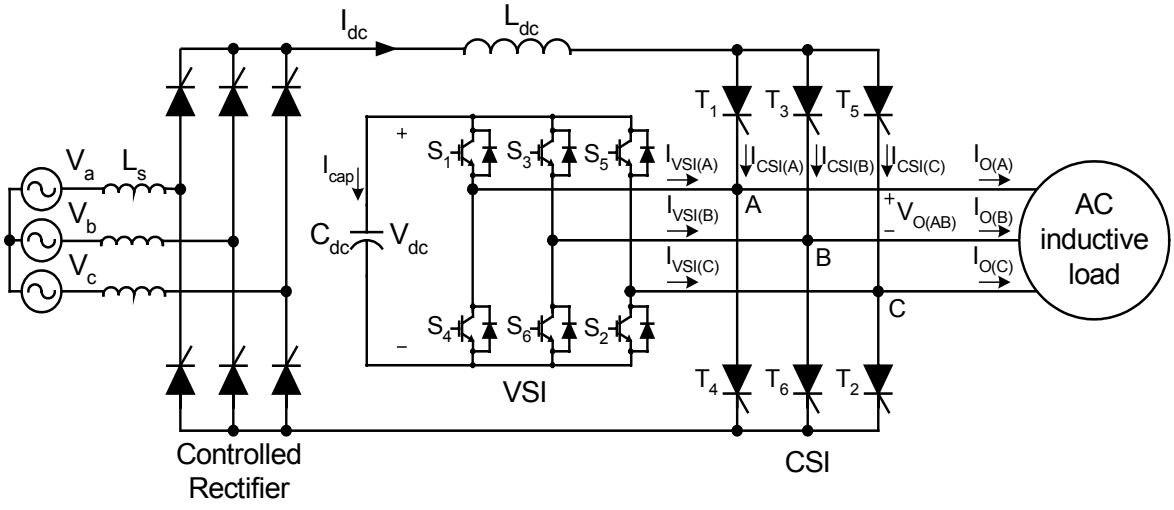


Fig. 4.1 Circuit diagram of proposed CSI system.

During the commutation periods, the VSI imposes the reverse-biased voltage on an off-going thyristor to turn it off. In addition, the VSI allows the load reactive energy to transfer from an off-going phase to an on-coming phase by absorbing and recovering the reactive energy through the dc capacitor. As a result, the load currents in the off-going phase and the on-coming phase gradually decrease and increase, respectively. Most of the load currents are supplied by the CSI, whereas the VSI currents represent a very small fraction of the total load currents because the VSI works only during the commutation intervals. Therefore, the VSI with much smaller power rating than the CSI can be adopted in the proposed scheme. The VSI performs three functions in the proposed CSI configuration:

- Turning off the thyristors in the CSI

At every commutation instant of the CSI, the VSI applies the reverse-biased dc voltage across an off-going thyristor for the short time duration, to turn off the thyristors. Therefore, the thyristors in the CSI can successfully turn off, based on the dc voltage stored in the VSI dc capacitor. Because this turn-off process of the thyristors is executed through the gate-turn-off switches in the VSI, the proposed CSI is free from any possible commutation failure of the thyristors. Furthermore, the VSI allows simple turn-off process of the thyristors by the VSI active switching without any complex commutation process.

- Transfer of the reactive load energy

The inductive load current and the corresponding reactive energy in the inductive loads like induction motors cannot instantaneously change. Thus, after turning off thyristors in the CSI, external devices and circuits must provide conduction paths of the load currents to decay the load leakage energy to zero. In the proposed topology, the VSI provides the current paths to gradually increase and decay the load currents during the load current commutation. The dc capacitor absorbs the reactive energy from the off-going load phase and recovers the energy to the on-coming load phase. As a

consequence, the load reactive energy is transferred from the off-going phase to the on-coming phase via the VSI.

This energy transfer process is divided into two stages, called “active energy-transfer stage” and “freewheeling energy-transfer stage”. During the active energy-transfer stage, the VSI is switched ON to allow the off-going load phase current to gradually decrease by applying the negative dc voltage to the phase. On the other hand, the on-coming phase is connected to the positive dc voltage to increase the on-coming load phase current with the same rate as the off-going load phase current decreases. During this stage, the dc capacitor transfers its energy to the on-coming load phase by discharging its energy. This stage is achieved by the active switching operation of the VSI, and the load currents are flown through the active switches of the VSI. Because this stage is executed prior to the thyristor turn-off process, the thyristors are turned off with the reduced load current. Therefore, the peak voltage stresses of the thyristors can be also reduced [44], [45].

During the freewheeling energy-transfer stage, all switches in the VSI turn off. However, the remaining load reactive currents will flow through the freewheeling diodes in the VSI. The on-coming phase current gradually increases to the dc-link current I_{dc}, while the off-going phase current decays to zero. The leakage energy of the off-going load phase is delivered to the dc capacitor in the VSI, and thereby, the capacitor is charged. In steady-state condition, two stages are balanced, and accordingly, about half of the load reactive energy is transferred during each stage. The dc voltage in the VSI is also maintained to the constant voltage level at steady state.

- Clamping of voltages across the load terminals and the thyristors

The dc capacitor in the VSI serves as a voltage clamper. The peak line-to-line voltage across the loads and the peak voltage stresses of the thyristors are limited to the VSI dc voltage. The dc voltage can be controlled with the time duration of the active energy-transfer stage. As a result, the peak load terminal voltage and the peak thyristor voltage stresses can be also adjusted through the VSI operation. Therefore, the excessive

high-voltage stresses on the load terminals and the thyristors can be avoided. The operational principle and process are, in detail, explained in the next section.

The proposed CSI topology looks similar to the hybrid converter structure proposed in Chapter III. However, the operational principle and control of two systems are quite distinct. Comparisons of two configurations are illustrated in Table 4.1.

Table 4.1 Comparison of two systems in Chapter III and IV.

	Hybrid converter in Chapter III	Advanced CSI in Chapter IV
Load current waveform	Sinusoidal waveform	Trapezoidal waveform
Load voltage waveform	Sinusoidal waveform	Non-sinusoidal waveform
Commutation type of thyristors	Natural commutation	Forced commutation
VSI operation	Continuous operation	Discontinuous operation
VSI function	▪ LCI commutation ▪ Reactive/harmonic current compensation	CSI commutation
VSI power rating	Large	Small
Isolated rectifier for VSI	Required	Not required
Output LC filter	Required	Not required

4.2.2 Operation principle

Figure 4.2 illustrates the operation modes of the proposed CSI with the current flow paths. In Fig. 4.2, the proposed system executes current commutation from the load

phase *A* to *B*, by turning off the thyristor T_1 and turning on T_3, with T_2 on. Corresponding equivalent circuits of each mode are also depicted. The CSI and the VSI are represented with the current source I_{dc} and the dc capacitor C_{dc} in the equivalent circuits, respectively.

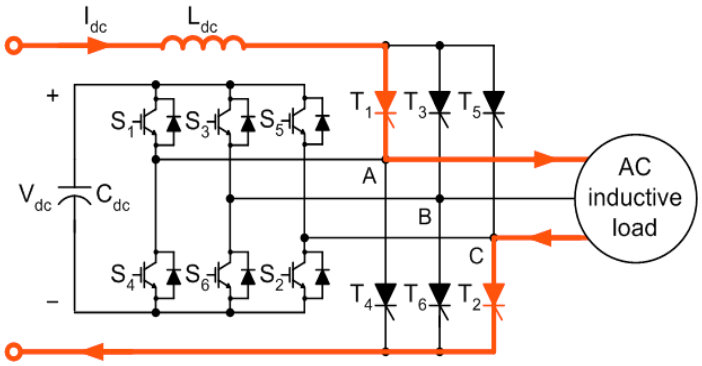
4.2.2.1 Mode 1

Mode 1 in Fig. 4.2(A.1) shows a steady-state condition with the load phases *A* and *C* conducted. The thyristors T_1 and T_2 in the CSI are on. During this non-commutating period, all switches in the VSI are off so that no current flows into the VSI. The equivalent circuit of the mode 1 is depicted in Fig. 4.2(A.2). Since the VSI dose not work during this non-commutating period, it does not appear across the load terminal. All the load currents are supplied through the CSI.

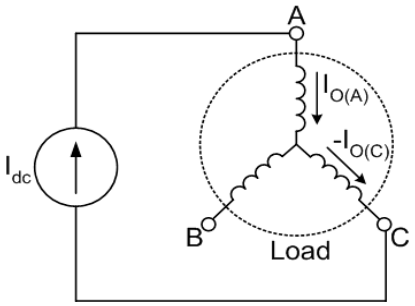
4.2.2.2 Mode 2: Active energy-transfer stage

The commutation process from phase *A* to *B* starts with mode 2, as seen in Fig. 4.2(B.1). The purpose of the mode 2 is to decrease the off-going phase load current $I_{O(A)}$ and increase the on-coming phase load current $I_{O(B)}$, with active VSI switching. For this purpose, S_3 and S_4 of the VSI are turned on. As a result, the negative and the positive dc voltage of the VSI are applied to the off-going phase *A* and the on-coming phase *B*, respectively. This polarity of the dc voltage forces $I_{O(A)}$ to decrease and $I_{O(B)}$ to increase, respectively. During this period, the VSI provides the current path from the off-going phase *A* to the on-coming phase *B* through the dc capacitor, with S_3 and S_4 on. The dc-link current I_{dc} through the thyristor T_1 is split from the load phase *A* to the phase *B* through the VSI. The on-coming phase current $I_{O(B)}$ increases exactly as much as the off-going phase current $I_{O(A)}$ declines. Thus, the sum of the two load currents in the on-coming and the off-going phases is equal to the dc-link current as

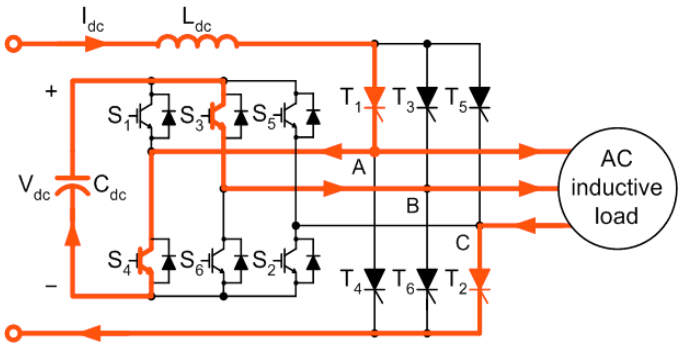
$$I_{O(A)} + I_{O(B)} = I_{dc} \tag{4.1}$$



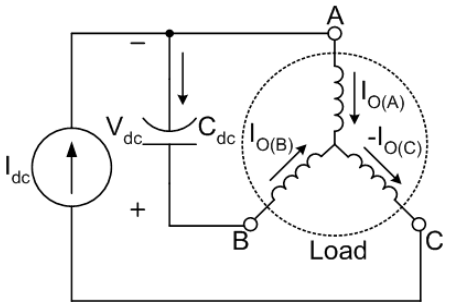
(A.1) mode 1



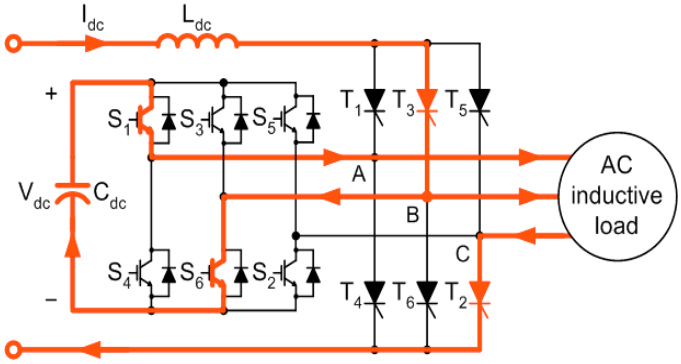
(A.2) equivalent circuit of mode 1



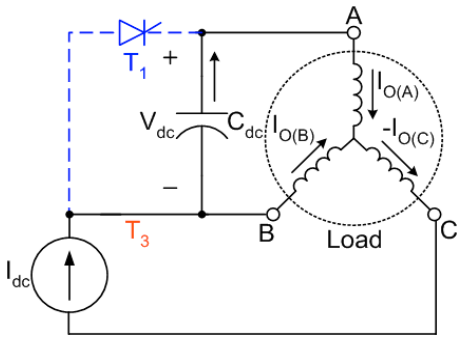
(B.1) mode 2



(B.2) equivalent circuit of mode 2

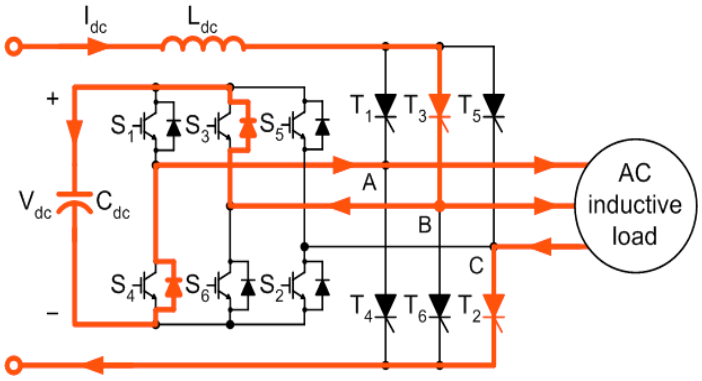


(C.1) mode 3

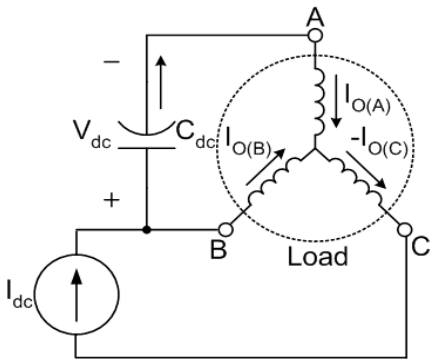


(C.2) equivalent circuit of mode 3

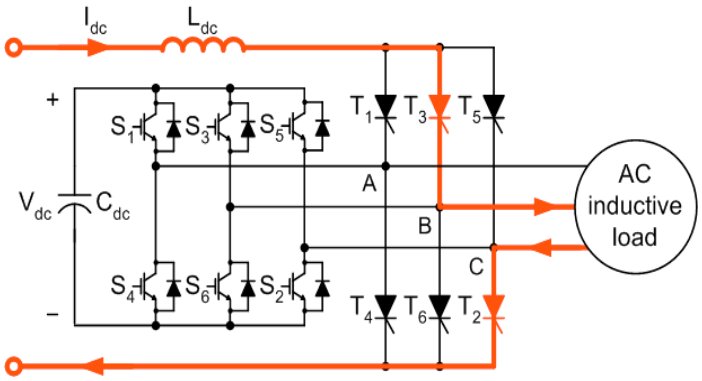
Fig. 4.2 Commutation modes and equivalent circuits of the proposed CSI during commutation from T_1 to T_3.



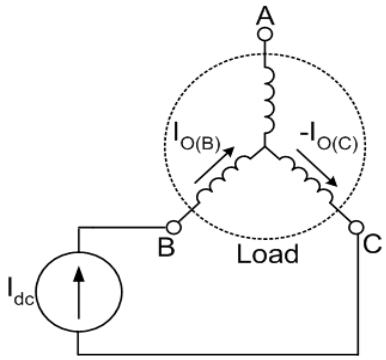
(D.1) mode 4



(D.2) equivalent circuit of mode 4



(E.1) mode 5



(E.2) equivalent circuit of mode 5

Fig. 4.2 Continued

In steady-state condition, the on-coming phase current $I_{O(B)}$ increases from zero to about half of the dc-link current I_{dc}, at the end of this mode. In the meantime, the off-going phase current $I_{O(A)}$ decreases to about half of the dc-link current. The dc capacitor C_{dc} discharges and the on-coming phase current $I_{O(B)}$ rises with the discharging energy of the dc capacitor. Figure 4.2(B.2) shows the equivalent circuit of mode 2. The dc capacitor C_{dc} appears across the load terminal *A* and *B* by the VSI switch operation. It is seen that the dc capacitor energy is discharged into the on-coming load phase *B*. In other words, the reactive energy in the dc capacitor transfers to the on-coming load phase, contributing to an increase of the phase current $I_{O(B)}$. Since the load current and energy

are transferred through the active switching components, this mode is termed “active energy-transfer stage”.

4.2.2.3 Mode 3: Thyristor turn-off stage

After a certain time period, let’s say τ, the on-coming thyristor T_3 in the CSI is fired. In addition, S_1 and S_6 in the VSI together turn on in mode 3, as illustrated in Fig. 4.2(C.1). In this mode, the off-going thyristor T_1 is impressed with reverse voltage across the dc capacitor, and turns off with the voltage V_{dc}. After turning off T_1, the entire dc-link current I_{dc} switches to the on-coming thyristor T_3. On the other hand, the remaining energy in the load phase *A* continues to flow through the VSI. Similarly, the load current $I_{O(B)}$ cannot abruptly jump to I_{dc} with T_3 turned on. As a result, the difference between the dc-link current and the motor phase *B* current flows through the VSI, charging the dc capacitor of the VSI. It should be noted that, contrary to the mode 2, the negative and the positive dc voltage of the VSI are connected to the on-coming phase *B* and the off-going phase *A*, respectively. As a consequence, the off-going phase current $I_{O(A)}$ is increased and the on-coming phase current $I_{O(B)}$ is decreased. Because this load current variation is opposed to the desired variation, this mode needs to last for short period compared with the mode 2. In fact, the thyristors are turned off almost instantaneously with applied reverse voltage [1], and consequently, the mode 3 is driven for the minimum time length to turn off the thyristors. The equivalent circuit of the mode 3 is depicted in Fig. 4.2(C.2). The turning-off process of the off-going thyristor is completed during mode 3. However, the remaining reactive energy in the load drives mode 4.

4.2.2.4 Mode 4: Freewheeling energy-transfer stage

After short interval of mode 3, ε, mode 4 begins with all VSI switches turned off, as depicted in Fig. 4.2(D.1). However, the residual energy in the load leakage reactance provides the current path through the freewheeling diodes of the switches S_3 and S_4 of

the VSI, which were the active switches in the mode 2. This mode is called "freewheeling energy-transfer stage", because the load current and the reactive energy are transferred through the freewheeling diodes of the VSI. The dc capacitor of the VSI is charged and the capacitor voltage V_{dc} is increased in this mode. In fact, this mode is a spontaneous stage caused by the reactive load energy. It should be noted that the VSI operation in the mode 4 is a counterpart of the mode 2, in terms of the VSI current direction, the conducting devices, and the dc capacitor operation, as illustrated in Table 4.2.

Table 4.2 Counterpart operation of mode 2 and 4.

	Mode 2	Mode 4
Current conduction device of VSI	Active switches	Freewheeling diodes
DC capacitor	Discharging	Charging

The equivalent circuit of this mode is shown in Fig. 4.2(D.2). The dc voltage of the VSI has the same polarity with mode 2, connecting the positive and negative dc voltage to the on-coming phase *B* and the off-going phase *A*, respectively. Thus, this mode drives the off-going current $I_{O(A)}$ to decrease, while the on-coming current $I_{O(B)}$ to increase, the same as mode 2 does. The dc capacitor in the VSI is charged with the remaining reactive energy of the off-going phase *A*. This energy stored in the capacitor during this mode is used to increase the on-coming phase load current at the active energy-transfer stage of the next commutation period. In other words, the reactive energy stored in the dc capacitor in this mode is returned to the on-coming phase of the load during the next commutation interval. The dc capacitor in the VSI is used as a temporary energy storage device to transfer the load reactive energy from the off-going phase to the on-coming phase. As a consequence, the energy amount transferred in mode 2 and 4 is balanced independent of the time length τ by adjusting the dc voltage level.

4.2.2.5 Mode 5

Mode 4 ends when the load current and corresponding reactive energy in the off-going phase *A* diminish to zero. Accordingly, the on-coming load phase current $I_{O(B)}$ rises to the dc-link current I_{dc}. This leads to mode 5 in Fig. 4.2(E.1). Because all load energy has been transferred from the off-going phase to the on-coming phase, the VSI stops operation until the next commutation process. The CSI entirely deals with the load currents. The equivalent circuit of this mode is shown in Fig. 4.2(E.2).

During these modes, typical voltage and current waveforms of the proposed CSI are shown in Fig. 4.3.

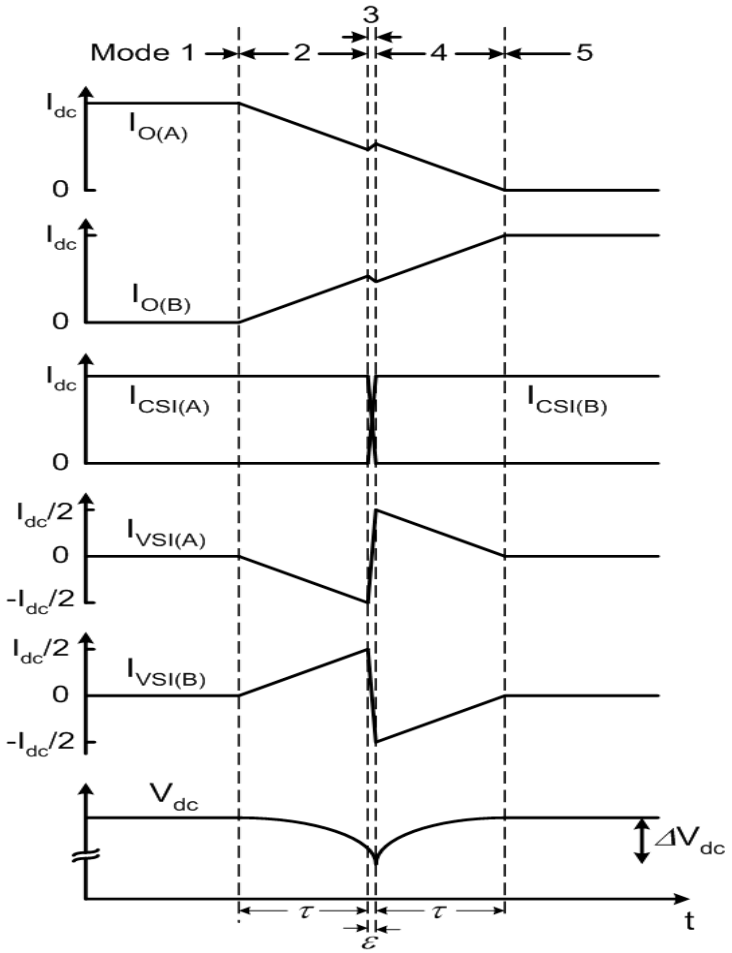


Fig. 4.3 Waveforms of the proposed CSI during commutation from T_1 to T_3.

4.2.3 Generalization of VSI control algorithm

The VSI control algorithm explained in the above section can be generalized, according to upper or lower thyristor transition in the CSI, in the Table 4.3.

Table 4.3 Generalized VSI control algorithm.

	Upper thyristor transition	Lower thyristor transition
Active Energy-Transfer Stage	• Lower VSI switch in a leg with an off-going thyristor : ON • Upper VSI switch in a leg with an on-coming thyristor : ON	• Upper VSI switch in a leg with an off-going thyristor : ON • Lower VSI switch in a leg with an on-coming thyristor : ON
Thyristor Turn-off Stage	• Upper VSI switch in a leg with an off-going thyristor : ON • Lower VSI switch in a leg with an on-coming thyristor : ON	• Lower VSI switch in a leg with an off-going thyristor : ON • Upper VSI switch in a leg with an on-coming thyristor : ON
Freewheeling Energy-Transfer Stage	• All VSI switches : OFF • Freewheeling diode of a lower VSI switch in a leg with an off-going thyristor : Current Conduction • Freewheeling diode of a upper VSI switch in a leg with an on-coming thyristor : Current Conduction	• All VSI switches : OFF • Freewheeling diode of a upper VSI switch in a leg with an off-going thyristor : Current Conduction • Freewheeling diode of a lower VSI switch in a leg with an on-coming thyristor : Current Conduction

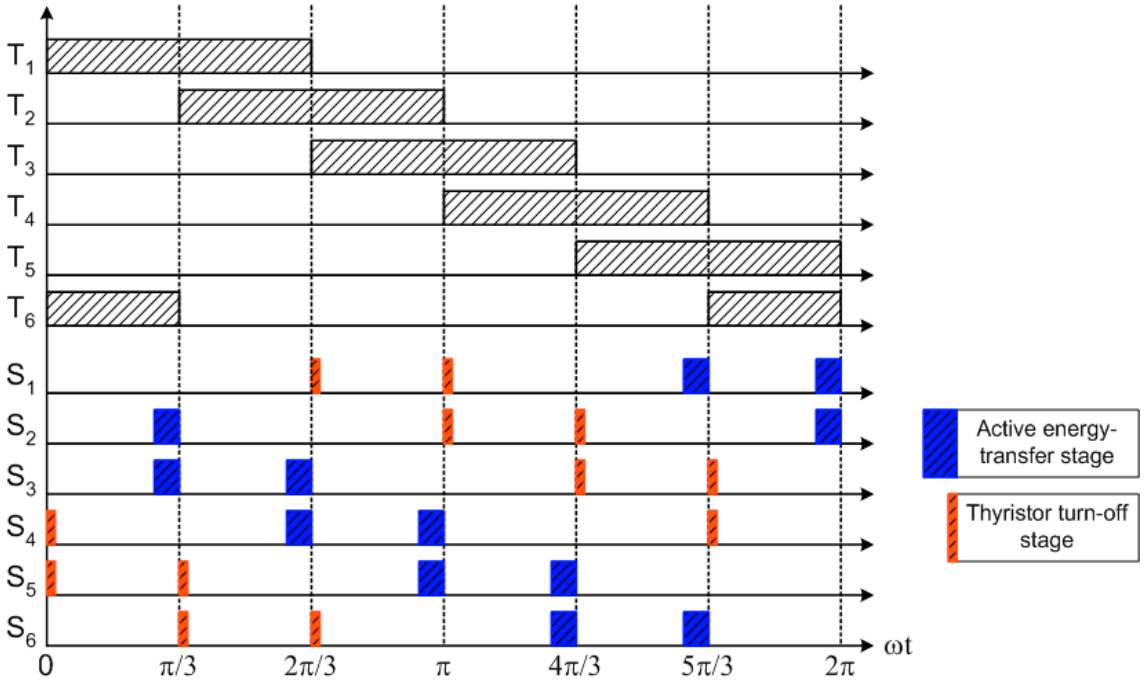


Fig. 4.4 Gate signals of the CSI and the VSI.

The gate commands of the CSI and the VSI are illustrated in Fig. 4.4. Note that the VSI gate commands are sequentially activated like the CSI gate signals.

4.2.4 VSI rating and dc capacitor voltage level

From cost point of view, it is desirable to employ a large CSI and a small VSI in the proposed CSI system. The thyristor-based CSI continuously operates to feed loads. On the other hand, the VSI works only during the commutation instants of the load currents. Therefore, the VSI rating is likely to be much smaller than the CSI. To investigate the VSI rating compared with the CSI rating, a rating factor η is defined with the ratio of the two inverter ratings. Because both the CSI and the VSI identically share the load phase voltage at the output terminals, the rating factor is directly proportional to the ratio of rms values of their output currents as

$$\eta = \frac{S_{VSI}}{S_{CSI}} = \frac{I_{VSI\ .rms}}{I_{CSI\ .rms}} \tag{4.2}$$

Assuming that the dc-link current I_{dc} as an ideal current source with no ripple components, the rms value of the CSI output current, $I_{CSI,rms}$ is given by

$$I_{CSI,rms} = \sqrt{\frac{2}{3}} I_{dc} \tag{4.3}$$

Because the time duration of the mode 3, ε, is negligible compared to τ, the rms value of the VSI current, $I_{VSI,rms}$ can be approximated by

$$I_{VSI,rms} = \sqrt{\frac{8}{T}\int_0^{\tau} I_{VSI}^2(t)\cdot dt} \tag{4.4}$$

From the VSI output current waveform in Fig. 4.3, it can be found as

$$I_{VSI,rms} = I_{dc}\sqrt{\frac{2}{3}\cdot\frac{\tau}{T_o}} \tag{4.5}$$

where, T_o is the period of the load output current. Therefore, the rating factor is given by

$$\eta = \sqrt{\tau \cdot f_o} \tag{4.6}$$

where, f_o is the output frequency of the load current.

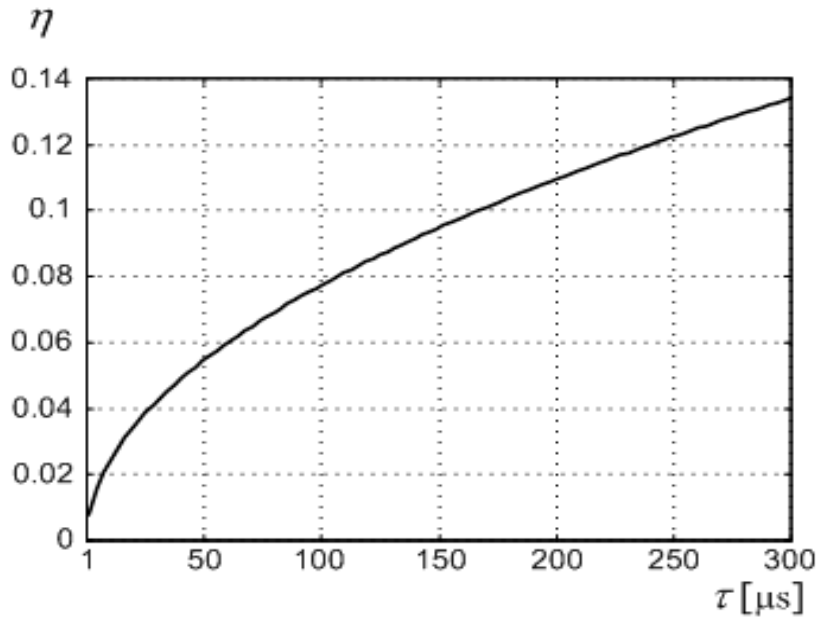


Fig. 4.5 Rating factor versus time interval of mode 2, τ (f_o =60Hz).

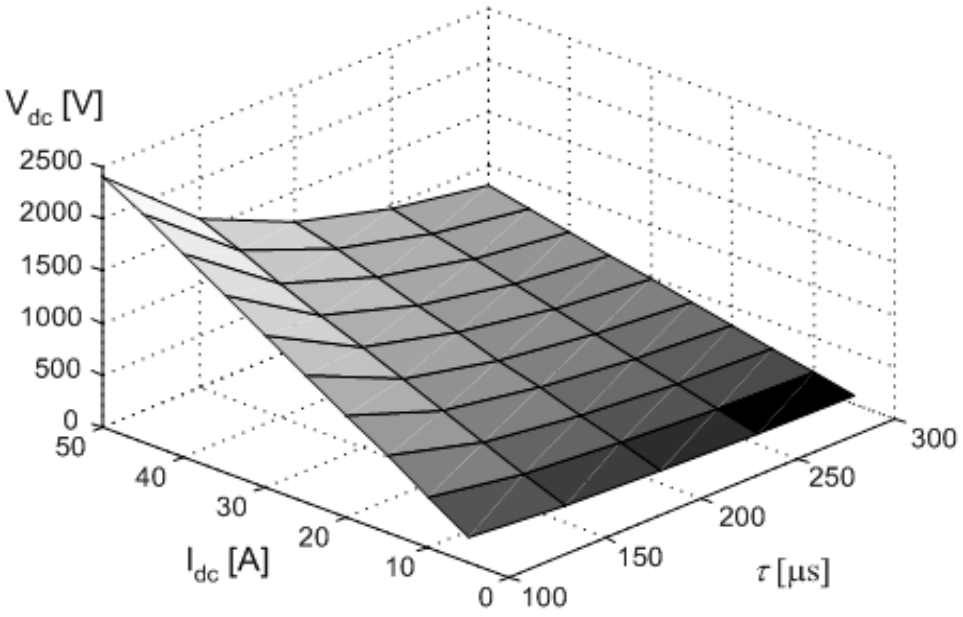


Fig. 4.6 VSI dc voltage level as a function of dc-link current and τ (f_o=60Hz, C_{dc}=100μF, R_{load}=3Ω, and L_{load}=5mH).

Figure 4.5 illustrates the rating factor as a function of τ. It can be seen that the VSI rating is less than about 13% of the CSI rating with the considered time length of mode 2. Figure 4.6 shows the dc voltage level of the VSI as a function of dc-link current and the time duration of mode 2. The dc capacitor voltage is increased with the reduced time duration of mode 2. It is due to the fact that the fast energy transfer over the short period τ results in the rising voltage of the dc capacitor [44]. In addition, the dc capacitor voltage is almost linearly proportional to the dc-link current I_{dc}, which is load current amplitude. The reason is that, given time period τ, the higher reactive energy trapped in the load inductance due to higher I_{dc} is returned into the dc capacitor, leading to the increased dc capacitor voltage. It can be seen that the dc voltage level can be controlled through adjusting the time length of mode 2, τ, resulting in the appropriate selection for the voltage rating of the VSI switching devices.

4.3 Simulation results

The proposed CSI system was simulated using a 12-hp induction motor to investigate the feasibility of the proposed topology and control principle. The output frequency was set at 60 Hz. Figure 4.7 shows the current and voltage waveforms of the proposed CSI. It is seen that the commutations of load current and turning off the thyristors are obtained based on the VSI operation. The load current smoothly changes during commutation periods due to the energy-transfer by the VSI. On the other hand, the CSI commutation is executed based on VSI switching operation, imposing the dc capacitor voltage in the reverse-biased direction for very short interval, ε. It is seen that mode 3 to turn off the thyristors is very short, compared with mode 2 and 4.

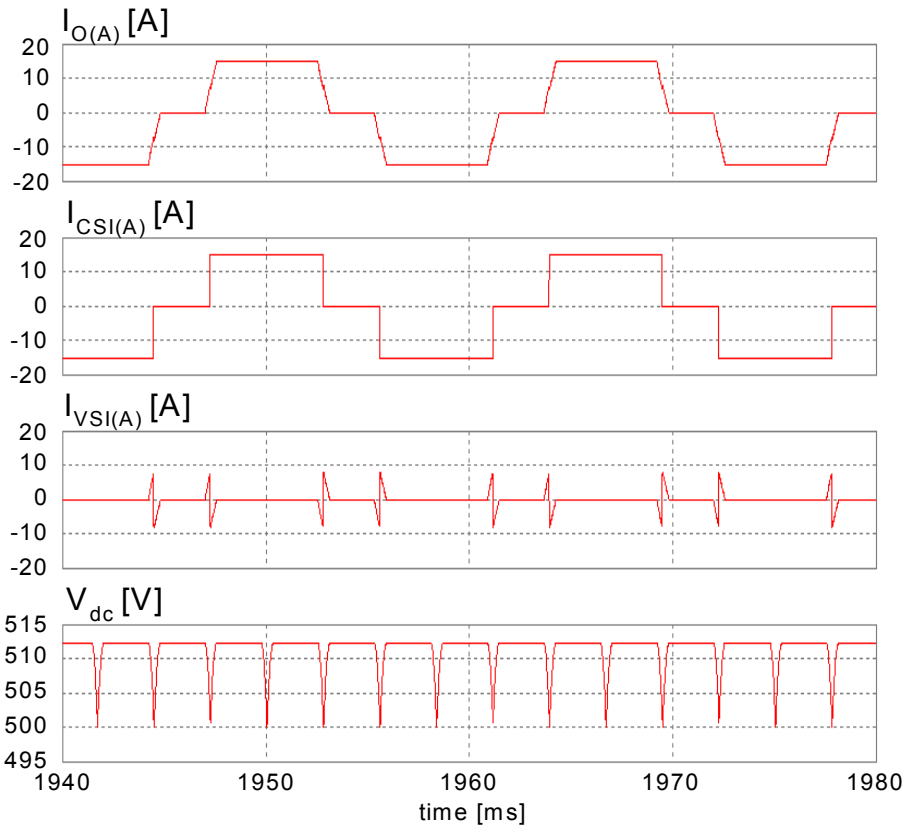


Fig. 4.7 Current and voltage waveforms of the proposed CSI (a) load current (b) CSI output current (c) VSI output current (d) dc capacitor voltage.

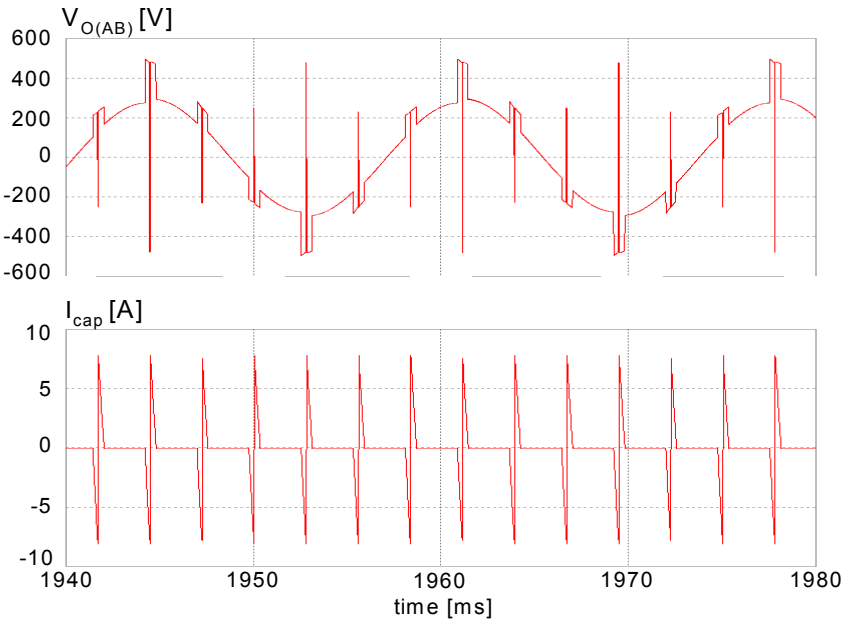


Fig. 4.8 Voltage and current waveforms of proposed CSI
(a) line-to-line load voltage (b) dc capacitor current.

During commutation periods of the load current, the VSI output current flows to allow the current paths for the load currents. As a result, the load current is gradually decrease and increase, and accordingly, the load reactive energy is transferred. The VSI output current is zero during the non-commutation periods of the load current. The VSI dc capacitor voltage discharges and charges to transfer the reactive load energy from the off-going phase to the on-coming phase during the commutation instants. A 100μF dc capacitor was used for this simulation. With a larger dc-link capacitor, the variation of the capacitor voltage for the commutation periods is reduced. It is observed that the dc capacitor voltage level is maintained to a constant value due to balanced effect of charging operation of mode 2 and discharging operation of mode 4. This voltage level can be controlled through adjusting the time duration of mode 2, τ, which can be controlled by the VSI. In this simulation, the time interval τ was set to 180 μsec, which yields that VSI rating is about 10% of the CSI rating. The line-to-line load voltage is illustrated in Fig. 4.8. As seen in the equivalent modes in Fig. 4.2, the load line voltage is determined by the CSI for the non-commutation periods. Meanwhile, during the

commutation periods, the dc capacitor voltage of the VSI appears across the line-to-line load terminals. The mode 2 and 4 impose the same dc capacitor voltage on the load voltage. However, the load voltage is reversed at the mode 3, in order to apply the dc capacitor voltage in the reverse-biased polarity across the off-going thyristors. The dc capacitor current is also depicted in Fig. 4.8. The capacitor current is balanced through the charging and discharging operations of the dc capacitor during the commutation periods.

4.4 Experimental results

To validate the proposed CSI topology and control algorithm, experimental results are shown in this section. The prototype experimental setup is composed of the CSI and the controlled rectifier based on thyristors (Motolora MCR16N), and the IGBT-based commercial VSI. The dc-link inductance for the CSI used in the experiment was 120 mH. A general-purpose induction motor with 230V, 60 Hz, and 1 hp was employed as the load. The proposed control structure has been implemented on the fixed-point digital signal processor (DSP) TMS320LF2407.

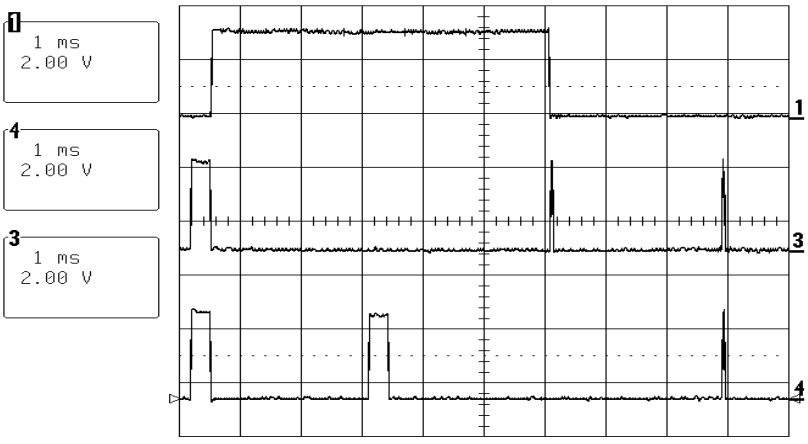


Fig. 4.9 Gate control signals for CSI thyristor *T1* (upper trace), VSI IGBT *S1* (middle trace), and *S2* (lower trace) from the DSP.

Figure 4.9 exhibits the control signals for the CSI thyristor *T1*, and the VSI IGBTs *S1* and *S2*, from DSP ports. The gate signals for the VSI IGBTs consist of long and short pulses corresponding to the active energy-transfer stage and the thyristor turn-off stage, respectively. The load current and the CSI output current waveforms are illustrated in Fig. 4.10. The load current is equal to the CSI output current for non-commutation periods. During commutation instants, the load current smoothly increases or decreases due to energy transfer operation of the VSI. On the other hand, the CSI output current instantaneously commutates based on the VSI dc voltage for the short thyristor turn-off stage. Figure 4.11 shows the load current and the VSI output current. It is seen that the VSI output current flows only during commutation periods. This VSI current allows transferring the reactive load energy. The VSI dc voltage is depicted with the load line voltage in Fig. 4.12. During non-commutation periods, the dc voltage is constant because of no current through the VSI. For commutation instants, the dc voltage discharges and charges due to the transfer operation of the reactive load energy. With the contrary effects of the active and the freewheeling energy-transfer stages, the dc voltage level is balanced.

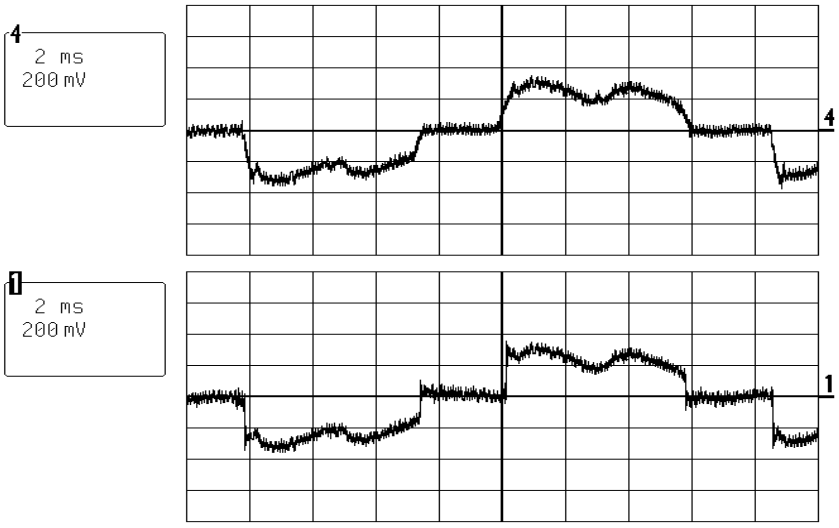


Fig. 4.10 Load current (upper trace: 1A/div) and
CSI output current (lower trace: 1A/div).

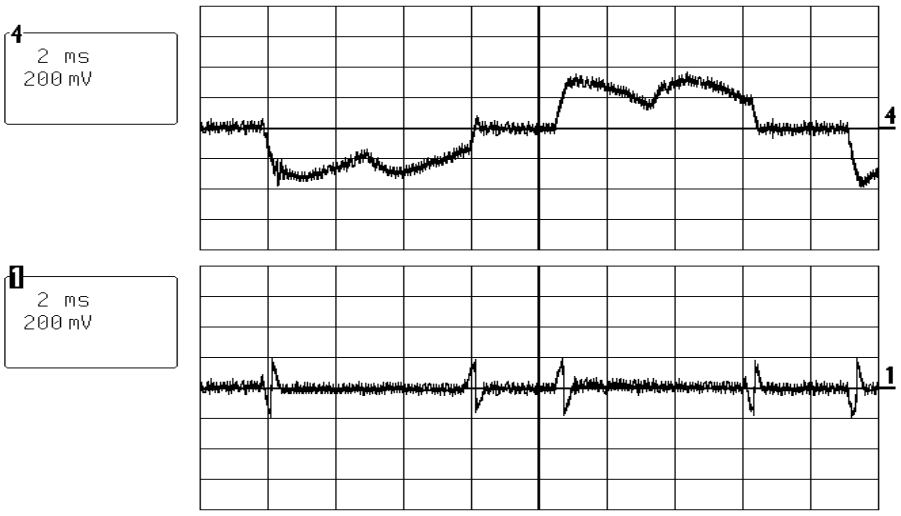


Fig. 4.11 Load current (upper trace: 1A/div) and
VSI output current (lower trace: 1A/div).

The load line voltage is also determined by the CSI output current. The load voltage is also disturbed with the dc voltage value during commutation periods. The peak values across the load voltage and the thyristor are limited to the VSI dc voltage. Figure 4.13 illustrates the supply voltage and the supply current. The dc-link current waveform regulated by the controlled rectifier is illustrated in Fig. 4.14.

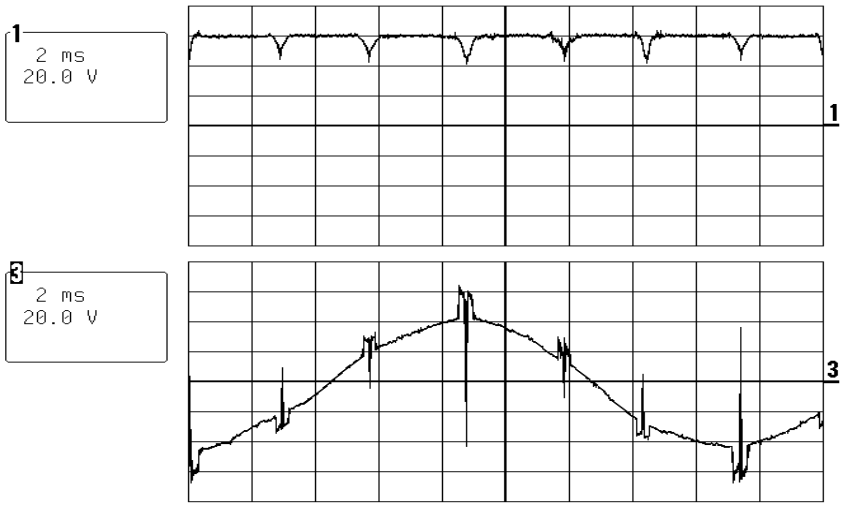


Fig. 4.12 VSI dc capacitor voltage (upper trace) and load line voltage (lower trace).

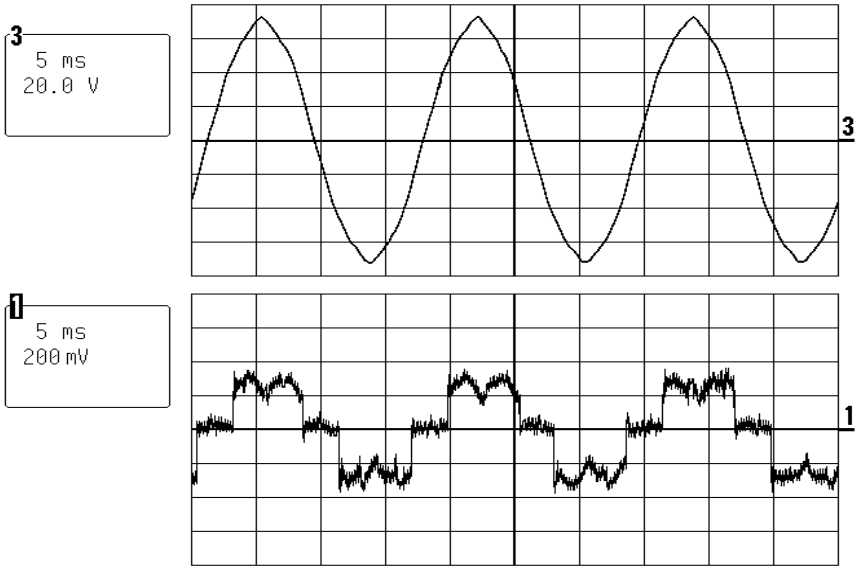


Fig. 4.13 Supply voltage (upper trace) and supply current (lower trace: 1A/div).

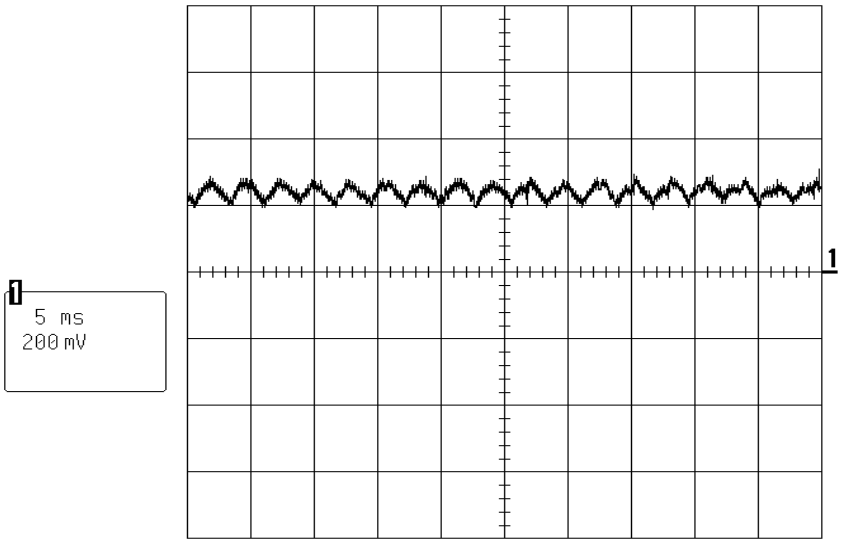


Fig. 4.14 DC-link current (1A/div).

4.5 Conclusion

This chapter has presented a forced-commutated CSI based on the thyristors, employing a small VSI as an external circuit. The VSI serving as a forced commutation circuit operates only during commutation periods of the load currents, and stops working the non-commutation intervals. Thanks to its discontinuous operation, the power rating of the VSI is greatly reduced, compared to the hybrid converter in chapter III, where the VSI continuously works to provide reactive and harmonic power.

During commutation instants of the load current, the VSI turns off the thyristors in the CSI as well as transfers the reactive load energy from the off-going phase to the on-coming phase. The off-going thyristors turn off with the VSI dc capacitor voltage imposed in the reverse-biased direction. In addition, the reactive energy of the off-going phase is temporarily stored in the dc capacitor of the VSI, and then, transferred to the on-coming phase during the load current commutation. The thyristor turning-off and the energy-transfer processes are easy and simple due to the VSI operation using the self-controlled devices. The peak voltages across the load and the thyristors are limited to the dc capacitor voltage level of the VSI, which can be also adjusted by the VSI operation. The feasibility of the proposed CSI system was verified by the computer simulation and the experimental results.

CHAPTER V

ANALYSES AND COMPARISONS OF TWO CONVERTER TOPOLOGIES WITH UNITY POWER FACTOR AND MULTIPLE AC/AC CONVERSIONS*

5.1 Introduction

Two topologies in Figs. 1.12 and 1.13, utilizing the PWM-VSR and the MFC, were introduced to reduce the cost and size of the utility-interface converters as well as realize multiple ac load controls in modern complex systems. Simplified configurations of two systems are illustrated in Figs. 5.1 and 5.2, where the PWM-VSIs and the ac loads are replaced with output load resistors. From *external* input/output terminal point of view, both topologies can show equal performances to provide not only unity power factor for the utility grid, but also independent power sources for output loads. However, a comparative study between the two types of topological systems until now is missing in the literature. The purpose of this chapter is to assess which topology can be a better choice in certain applications, by clearly addressing and comparing the *internal* features and requirements of the two systems. For the fundamental question, the chapter analyzes the two topological systems with only external terminal constraints. These terminal constraints are that the sinusoidal supply voltages and currents operating at unity power factor are defined, and a total output power is specified. In order to achieve a fair comparison, it is assumed that both systems are designed to run on equal balanced, three-phase grid supply (line-to-line voltage V_{LL}=460V and frequency f_g=60Hz) with unity power factor. The topologies are to meet the same total output power (P_{out}) requirement.

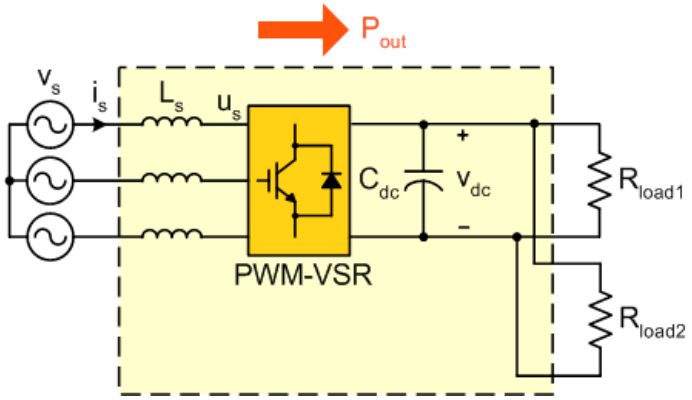


Fig. 5.1 PWM-VSR based topology with unity power factor and multiple loads.

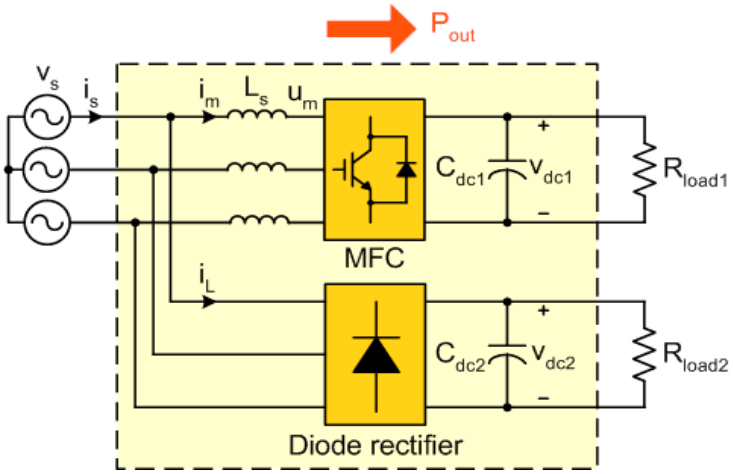


Fig. 5.2 MFC based topology with unity power factor and multiple loads.

One possible drawback of the MFC based topology in Fig. 5.2 is its limited regeneration ability since the diode rectifier with its unidirectional power flow characteristics prevents the regeneration of load energy. As a result, only the output power flown through the MFC can be regenerated to the supply. On the other hands, the PWM-VSR based topology in Fig. 5.1 provides a continuous operation for the regenerative loads due to the bi-directional power flow of the converter. Aside from the difference in regeneration ability, it is important to investigate the comparison between the two systems because not all ac loads require regeneration. Intuition suggests that the MFC size in Fig. 5.2 is likely to be lower because of the lower output power level it

needs to carry. This chapter first examines the question of converter sizes related to system topologies, by deriving systematic analyses and closed-form expressions. It is verified that although the MFC, in general, results in substantially smaller size than the PWM-VSR, this result can undergo a change in certain conditions. Having compared the converter sizes, the chapter, then tackles the issue of comparing the dc-link voltage requirement, semiconductor ratings and losses. Understanding that the reactive components used for energy storage and filtering constraint the cost and power density realizable in the converters, the reactive component comparisons of the two systems are included. Rigorous mathematical expressions based on quantified physical features and their operational interpretations are presented through theoretical derivations of two topologies.

5.2 Converter ratings

The objective in this section is to determine and find closed-form expressions for the converter kVA ratings of the two systems depicted in Figs. 5.1 and 5.2, given certain terminal constraints. Both converter configurations are with a filter inductor on the ac side of the circuits to boost a dc-link voltage over input line-to-line voltage and eliminate the switching frequency components. Therefore, both converters must supply the reactive power to the inductor, leading to the increase of the kVA ratings of the converters. With the input/output constraints, the effect of the input filter inductor is included.

5.2.1 PWM-VSR rating

Since the PWM-VSR (subsequently referred to as the VSR) in Fig. 5.1 has both sinusoidal current and voltage in its ac side, calculating its rating is straightforward. In order to find a closed-form expression for the VSR kVA rating, only the fundamental

components of the input voltage and current are considered. The supply phase voltage and current are

$$v_s(\omega t) = \sqrt{2}V_s \cos \omega t$$
$$i_s(\omega t) = \sqrt{2}I_s \cos \omega t \qquad (5.1)$$

where, V_s and I_s are the rms values of the supply phase voltage and current, respectively. The line-to-neutral supply voltage V_s is found by dividing the given V_{LL} by $\sqrt{3}$. With the constraints of unity power factor operation and no converter and inductor loss, the VSR kVA can be derived, from the rms voltage (u_s) and current (i_s) on the converter ac side, as

$$S_{VSR} = P_{out}\sqrt{1 + (\frac{\omega L_s P_{out}}{3V_s^2})^2} \qquad (5.2)$$

where, L_s denotes the input filter inductance. Equation (5.2) clearly shows that the VSR rating is decided by the output power and the input filter inductor. This is due to the fact that the converter delivers real power to its loads and reactive power to the filter inductor.

The filter effect becomes more apparent from the phasor diagram for the VSR operating with unity power factor shown in Fig. 5.3. In Fig. 5.3, given unity power factor constraint at the utility terminal, the input voltage (U_s) and current (I_s) on the ac side of the VSR have a γ degree phase shift, which shows a leading power factor. This implies that the unity power factor operation in the utility is achieved when the VSR operating with leading power factor properly cancels the lagging inductive VAR of the filter inductor. Thus, the input filter size should be kept small since a larger input filter leads to higher kVA requirement of the VSR. Figure 5.4 shows the kVA rating for the VSR as

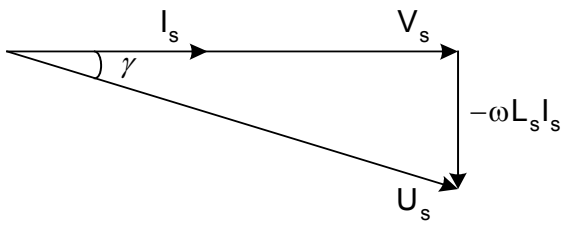


Fig. 5.3 Phasor diagram of VSR with unity power factor operation.

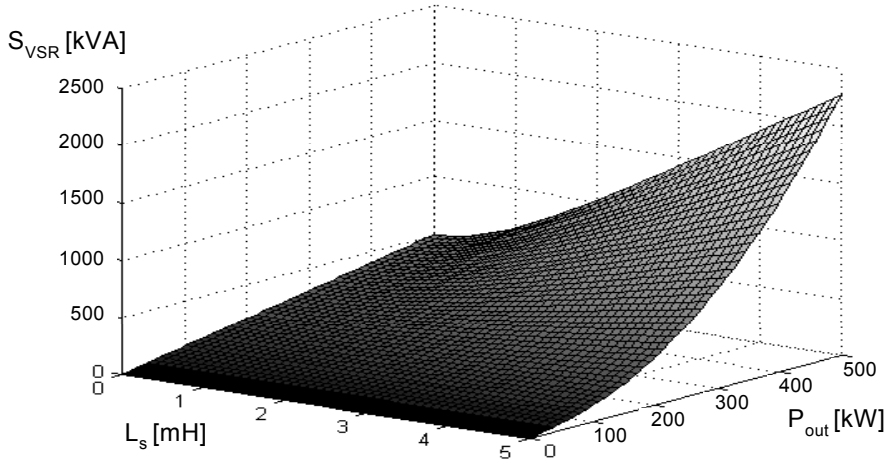


Fig. 5.4 VSR rating versus output power and input inductor (V_{LL}=460V and f_g=60Hz).

a function of the output power and the input filter size. The converter rating clearly increases with the increase in the output power and the filter inductance.

5.2.2 Multi-Function Converter (MFC) rating

The kVA rating of the diode rectifier in the system of Fig. 5.2 is not considered for the converter rating analysis, because the diode rectifier is not comparable to the MFC from cost point of view. The MFC size is, similar to the VSR rating, dependent to the output power to its load and its input filter inductance. In addition, the MFC kVA rating is likely to be influenced by the displacement factor and the distortion level of the diode rectifier current (i_L) since the MFC should compensate the reactive and harmonic powers generated by the diode rectifier.

In this study, before analyzing the MFC rating with a specific operating point of the diode rectifier, general properties of its rating related with a diode rectifier are examined, by initially assuming the ac-side filter L_s to be zero. This assumption eliminates the need to model the interaction of the MFC rating with the input filter inductor. This implies that the kVA rating of the MFC is only dependent on the distortion degree of the diode rectifier current such as the total harmonic distortion (THD) and the displacement factor, in conjunction with the output power level. It can

lead to the relationship between the MFC rating and various diode rectifier current features. The MFC rating analysis is then extended by including the effect of the input filter inductance, using a typical current waveform of the diode rectifier.

5.2.2.1 Analysis without input filter

By neglecting the input filter inductor L_s, a power flow model of the MFC based system shown in Fig. 5.2 can be depicted as in Fig. 5.5. It is shown that the MFC is handling the real power for its own load as well as the reactive and harmonic powers generated by the diode rectifier to keep the unity power factor at the grid terminal. The converter rating of the MFC and the diode rectifier from Fig. 5.5 is given by

$$\frac{S_{MFC}}{S_{diode\ \ rectifier}} = \frac{\sqrt{P_1^{\,2} + Q_2^{\,2} + H_2^{\,2}}}{\sqrt{P_2^{\,2} + Q_2^{\,2} + H_2^{\,2}}} \tag{5.3}$$

The supply current in (5.1) can be divided into two components for powers P_1 and P_2 which denote the output powers delivered through the MFC and the diode rectifier, respectively.

$$i_s(\omega t) = \sqrt{2}(I_{s1} + I_{s2})\cos \omega t \tag{5.4}$$

where, I_{s1} and I_{s2} describe the supply current components to deliver the output power P_1 and P_2, respectively.

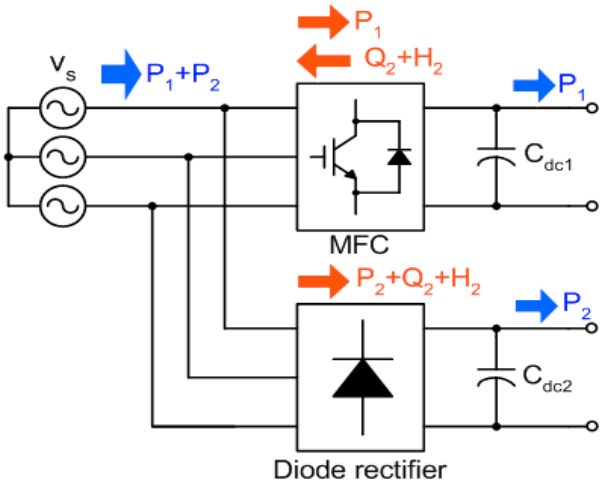


Fig. 5.5 Power flow model in MFC based topology without input filter.

The total output power, which this topology supplies, is given by

$$P_{out} = P_1 + P_2 \tag{5.5}$$

The real, reactive, and harmonic powers of the diode rectifier are given by [47],

$$P_2 = 3V_s I_{s2} \cos\varphi_1,\ Q_2 = 3V_s I_{s2} \sin\varphi_1,\ H_2 = 3V_s I_{s2} THD_{iL} \tag{5.6}$$

where, THD_{iL} and φ_1 denote the total harmonic distortion and the displacement factor angle of i_L, respectively. The expression for the MFC rating, from (5.3) and (5.6), is given by

$$S_{MFC} = \frac{P_2}{\cos\varphi_1}\sqrt{\sin^2\varphi_1 + THD_{iL}{}^2 + (P_1\cos\varphi_1 / P_2)^2} \tag{5.7}$$

Equation (5.7) shows that the MFC rating is influenced by several factors: displacement factor angle (φ_1) and THD_{iL} of the diode rectifier current as well as the output powers flown through the MFC and the diode rectifier. It is very important to note that the resultant MFC rating is dependent on the ratio of the output powers through the MFC (P_1) and the diode rectifier (P_2). In some applications, the MFC and the diode rectifier can equally split their output powers: $P_1 = P_2 = (1/2)P_{out}$. In this case, the MFC rating normalized by the total output power is given by

$$\frac{S_{MFC}}{P_{out}} = \frac{1}{2\cos\varphi_1}\sqrt{1 + THD_{iL}{}^2} \tag{5.8}$$

Figure 5.6 shows the plot of the MFC rating normalized by the total output power as a function of THD_{iL} and the displacement factor of the diode rectifier. The curve shows that the kVA rating of the MFC increases with increasing THD_{iL} and φ_1. This implies that if the THD and the displacement factor angle of the diode rectifier rise at constant output power, the MFC should compensate the higher reactive and harmonic powers, resulting in an increase of its rating. For the purpose of comparison, the VSR rating normalized with the total output power is displayed with the same assumption of L_s=0. Notice that the VSR rating is equal to the output power by neglecting the filter inductance in (5.2). Though the MFC rating connected with the diode rectifier with low THD_{iL} and small φ_1 is substantially lower than the VSR rating, severe distortion of the diode rectifier current yields a higher MFC rating than the VSR rating.

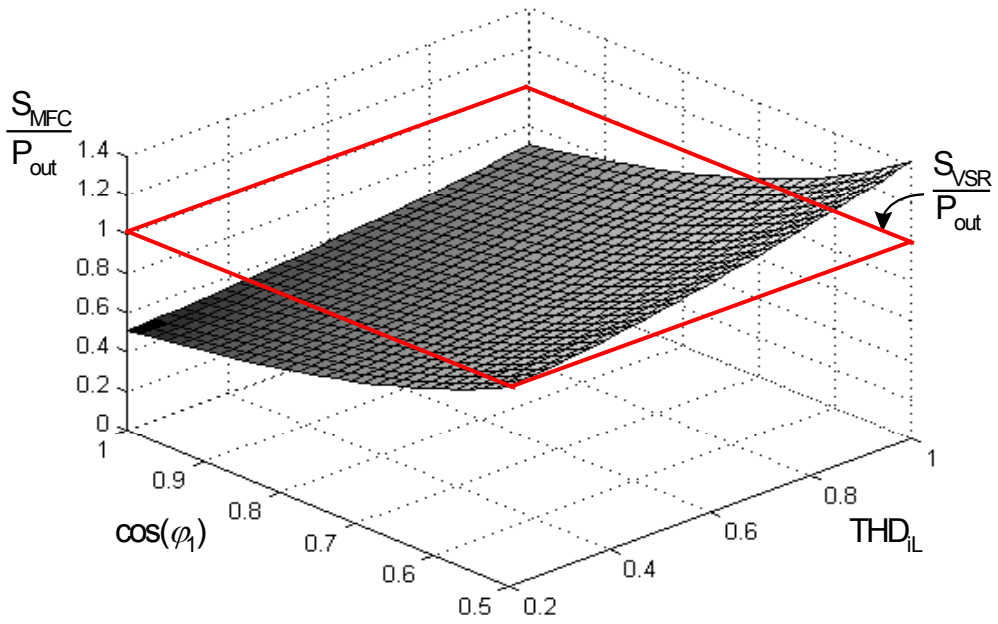


Fig. 5.6 MFC rating normalized by the output power for the condition of P_1=P_2.

Now, an output power split factor between the MFC and the diode rectifier, which can minimize the kVA rating of the MFC is derived [60]. An output power split factor k is defined as the ratio of the output power through the diode rectifier and the total output power as,

$$k = \frac{P_2}{P_{out}} \quad , \qquad \text{where } 0 \le k \le 1 \tag{5.9}$$

Note that the system structure with k=0 leads to the VSR topology and with k=1 yields an APF circuit. Therefore, all following MFC results can be utilized for APFs with unity value of k. With the defined k, the MFC rating is given by,

$$S_{MFC} = \frac{kP_{out}}{\cos\varphi_1}\sqrt{\sin^2\varphi_1 + THD_{iL}{}^2 + (\frac{1-k}{k})^2\cos^2\varphi_1} \tag{5.10}$$

Then the value of k, which minimizes the MFC rating, can be found by taking

$$\frac{dS_{MFC}}{dk} = 0 \tag{5.11}$$

This yields an optimized power split factor k_{op} given by

$$k_{op} = \frac{\cos^2 \varphi_1}{1 + THD_{iL}^{\ 2}} \tag{5.12}$$

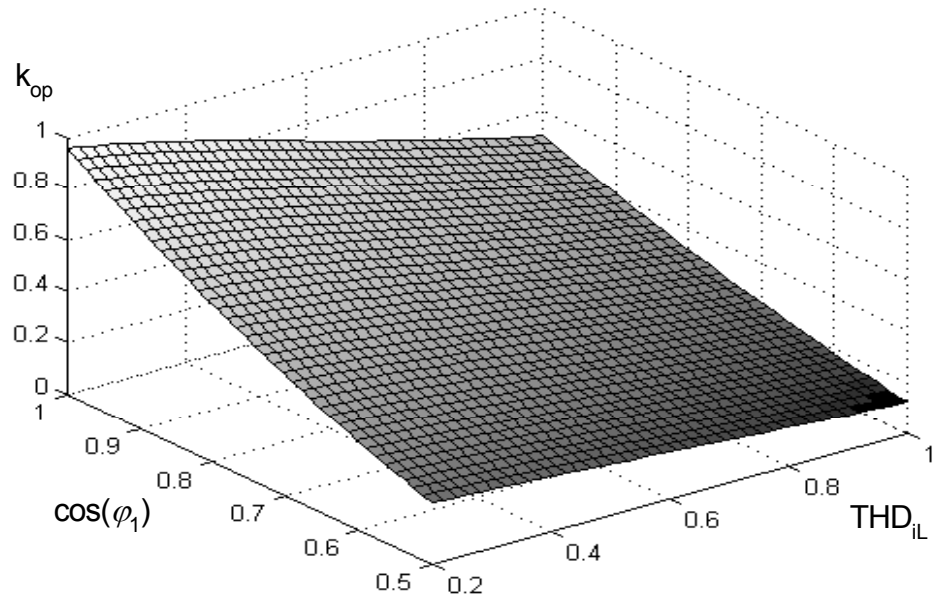


Fig. 5.7 Optimized power split factor as a function of THD_{iL} and φ_1.

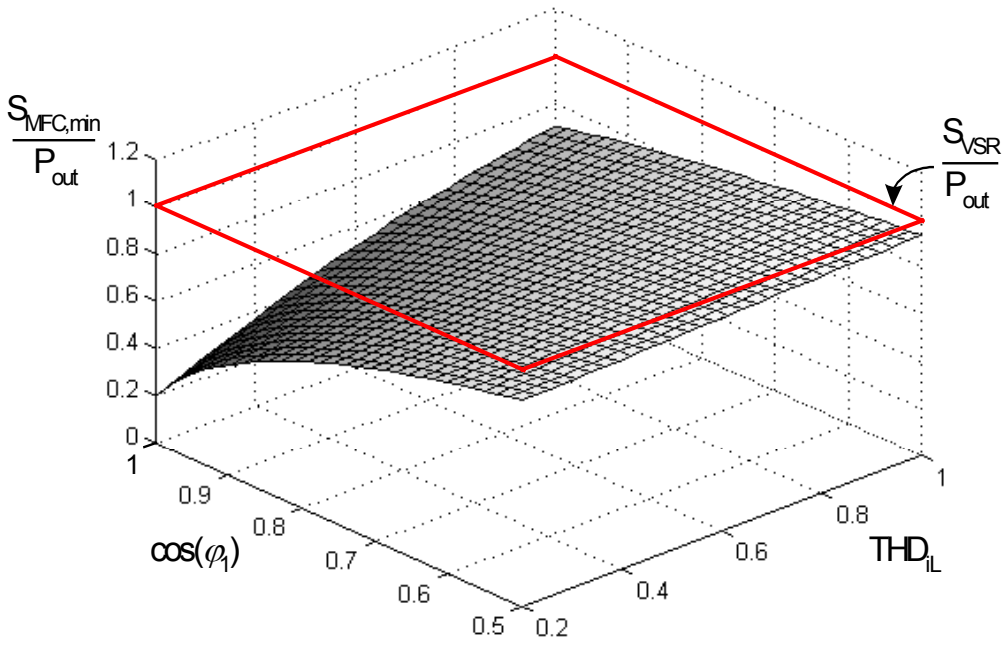


Fig. 5.8 Normalized minimum MFC rating versus operating points of the diode rectifier.

It is worth noting that from (5.12), with increased distortion level of the diode rectifier current (increasing THD_{iL} and φ_1), the optimized power split factor decreases, which yields more output power flown through the MFC. This is illustrated in Fig. 5.7 showing the plot of optimized power split factor k_{op} versus THD_{iL} and the displacement factor. Once the optimized power split factor is known, the minimum kVA rating of the MFC is

$$S_{MFC,\min} = P_{out}\sqrt{1-k_{op}} \tag{5.13}$$

It is important to note that a unique value of k_{op} and the corresponding unique minimum MFC rating exist at every operating point of the diode rectifier. Figure 5.8 shows a minimum MFC rating, $S_{MFC,min}$ with optimized split factor k_{op} as a function of the diode rectifier input current characteristics. It is seen that unlike the case of k=0.5, the normalized minimum kVA rating of the MFC is lower than the normalized VSR rating for all operating regions of the diode rectifier.

5.2.2.2. Analysis with input filter

The MFC rating with the input filter effect is expected to increase due to the fact that the converter has to additionally supply the reactive power to the input inductor as well as the reactive and harmonic powers to the diode rectifier. The following analysis for the MFC rating including the effect of the input inductor is based on the ideal six-pulse diode rectifier with the dc-side current I_{dc}, operating at unity displacement factor [2], [59]. Current commutations of the diode rectifier are assumed to be instantaneous. These assumptions yield values for the total harmonic distortion and displacement factor of the diode rectifier current as THD_{iL} = 0.31 and $\cos(\varphi_1)$ = 1. As before, assume that switching frequency components of the MFC current and voltage are negligible. Figure 5.9 shows the supply current, the MFC current, and the diode rectifier current in the case of k=0.5.

The kVA rating of the MFC is defined by

$$S_{MFC} = 3I_{m,rms}U_{m,rms} \tag{5.14}$$

where, $I_{m,rms}$ and $U_{m,rms}$ are the rms values of the MFC input current (i_m) and voltage (u_m), respectively. The MFC rms current is written by

$$I_{m,rms}{}^2 = I_{s1}{}^2 - I_{s2}{}^2 + I_{L,rms}{}^2 \tag{5.15}$$

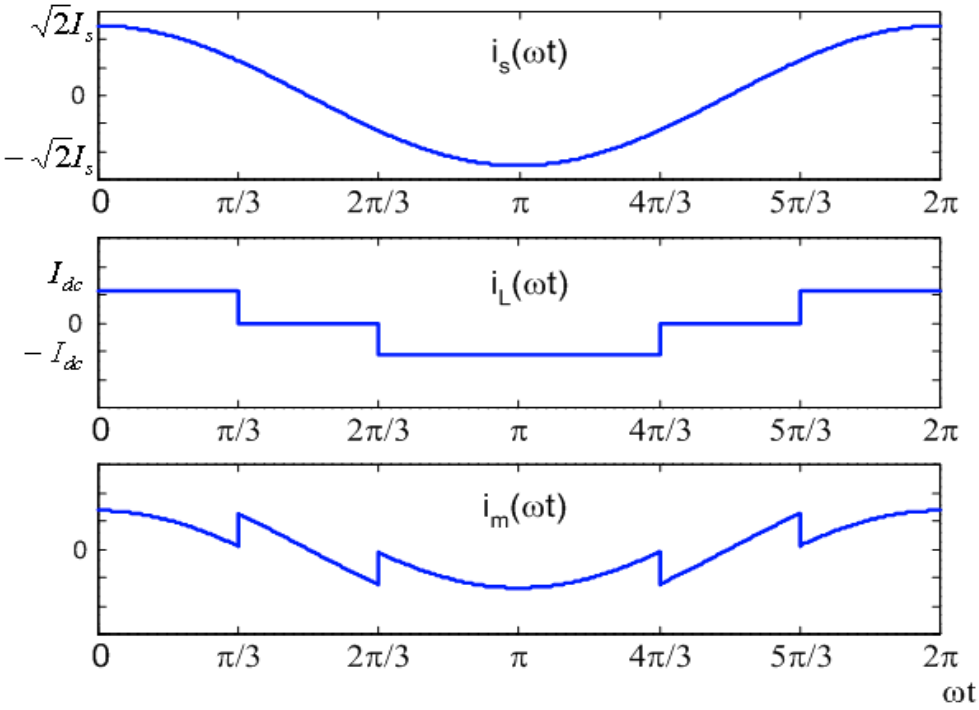


Fig. 5.9 Supply current, diode rectifier input current, and MFC input current with k=0.5.

where, $I_{L,rms}$ denotes the rms value of the diode rectifier current i_L. The supply rms currents are given by

$$I_{s1} = \frac{P_1}{3V_s} \quad , \quad I_{s2} = \frac{P_2}{3V_s} \tag{5.16}$$

The rms voltage of the MFC is also written by

$$U_{m,rms}{}^2 = \frac{1}{2\pi}\int_0^{2\pi}\left(v_s(\omega t) - \omega L_s \frac{di_m(\omega t)}{d(\omega t)}\right)^2 d(\omega t) \tag{5.17}$$

The MFC input current is expressed, by Fourier analysis, as

$$i_m(\omega t) = \sqrt{2}I_{s1}\cos(\omega t) + \frac{2\sqrt{3}}{\pi} I_{dc}\left(\frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t + \frac{1}{11}\cos 11\omega t \cdots\right) \tag{5.18}$$

Thus, the kVA rating of MFC can be derived, by reflecting (5.15) and (5.17) to (5.14), as

$$S_{MFC} = \sqrt{P_1^2 - (1-\frac{\pi^2}{9})P_2^2}\sqrt{1+(\frac{\omega L_s}{3V_s^2})^2(P_1^2+nP_2^2)} \tag{5.19}$$

where, n denotes the number of harmonic components to be canceled. By expressing each output power supplied through the MFC and the diode rectifier using the output power split factor defined by (5.9), the MFC rating is given by

$$S_{MFC} = P_{out}\sqrt{(1-k)^2 - (1-\frac{\pi^2}{9})k^2}\sqrt{1+(\frac{\omega L_s P_{out}}{3V_s^2})^2((1-k)^2+nk^2)} \tag{5.20}$$

It is noticed that the MFC rating is influenced by the input filter inductance, total output power, output power split factor, and the number of harmonics the MFC compensates. Note that in the case of k=0, the system of Fig. 5.2 changes into the VSR of Fig. 5.1, resulting in (5.20) equal to (5.2). The specification for the number of harmonic components to be canceled by the MFC can be set from the total harmonic distortion (THD_i) limitation of the supply current to meet IEEE 519 harmonic standards. IEEE 519 harmonic current limits are to be met up to the 50th harmonic in the supply current [46]. This results in n = 16, the supply current total harmonic distortion THD_{is} = 0.08, and the supply power factor pf = 0.997. However, THD_{is} should be suppressed to lower levels for special applications such as for hospital environments, yielding the increase of the number n.

Figure 5.10 shows the kVA rating of the MFC defined in (5.20) as a function of the output power split factor for several total output powers with V_{LL}=460V, L_s=0.5mH, and n=16. It is shown that the MFC kVA rating varies with the power split factor k given the total output power, yielding the possibility of determining an optimized power split factor k_{op}. It also shows that an optimized split factor, which yields a minimum MFC rating, decreases with the increasing total output power. Therefore, as before, the optimized power split factor k_{op}, which minimizes the MFC rating, can be found and the corresponding minimum MFC rating is also obtained by reflecting the k_{op} into (5.20). It is apparent that the optimized split factor k_{op} is a function of input inductance L_s, total output power P_{out}, and the number of compensating harmonics n. These relationships are

illustrated in Figs. 5.11 and 5.12 with different parameters. It is important to notice that a unique optimized split factor and a corresponding unique minimum converter rating, here again, exist given P_{out}, L_s, and n.

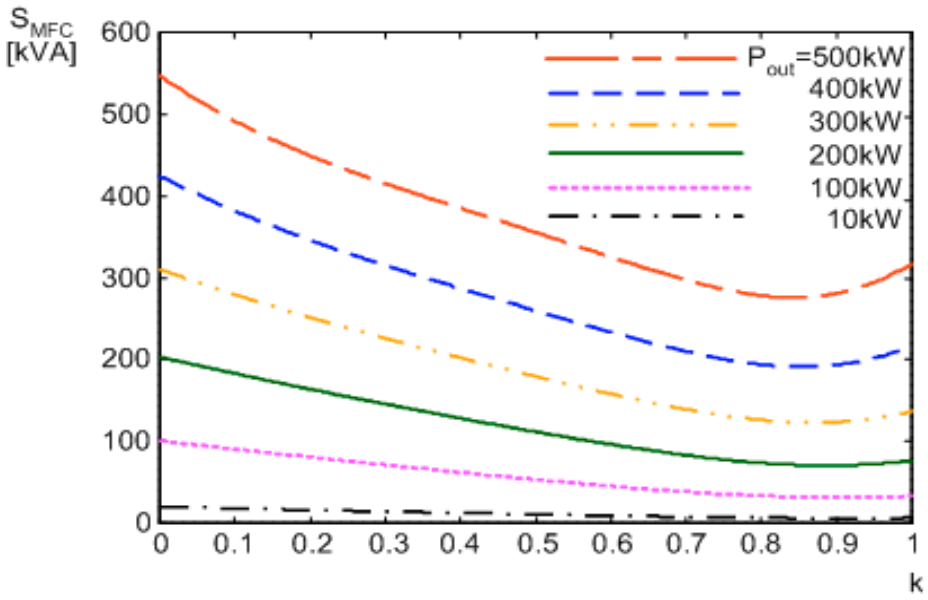


Fig. 5.10 MFC rating versus output power split factor (V_{LL}=460V, n=16, and L_s=0.5mH).

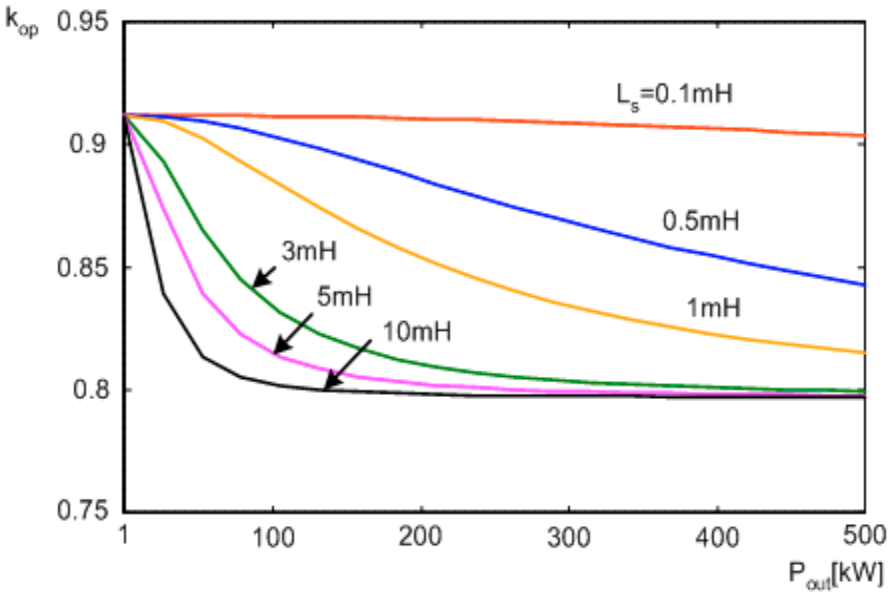


Fig. 5.11 Optimized power split factor versus output power (V_{LL}=460V and n=16).

Figure 5.11 shows a plot of the optimized split factor k_{op} versus output power for several filter inductor values. The optimized factor, k_{op}, is decreased by the increase of the filter inductor size for the specified output power.

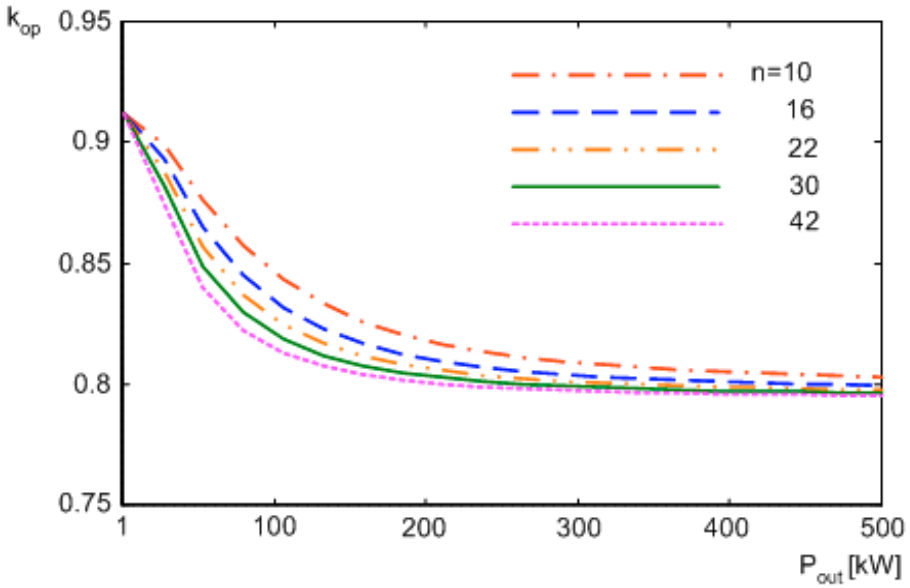


Fig. 5.12 Optimized power split factor versus output power (V_{LL}=460V and L_s=3mH).

Figure 5.12 shows a plot of the optimized power split factor as a function of output power for several values of n. The optimized factor k_{op} decreases with increasing n, which results in higher harmonic power from the MFC to the diode rectifier. Thus, the optimized split factor decreases with the increasing output power, input inductor size, and the number of harmonic components. This implies that the MFC rating can be minimized by letting more output power delivered through the MFC as the output power, the input inductor, and n are increased. Notice that the k_{op} is reached to around 0.8 with the increase of L_s, n, and P_{out} in Figs. 5.11 and 5.12, because this analysis assumed that THD_{iL} and φ_1 of the diode rectifier current take on 0.31 and 0, respectively. For applications with a diode rectifier with higher value of THD_{iL} and φ_1, the optimized split factor will be less than 0.8 as seen in Fig. 5.7.

Figure 5.13 shows the converter ratings of the VSR (k=0), the MFC with k=0.5, the MFC with k_{op}, and the APF (k=1) based on the output power for n=16 and L_s=3mH.

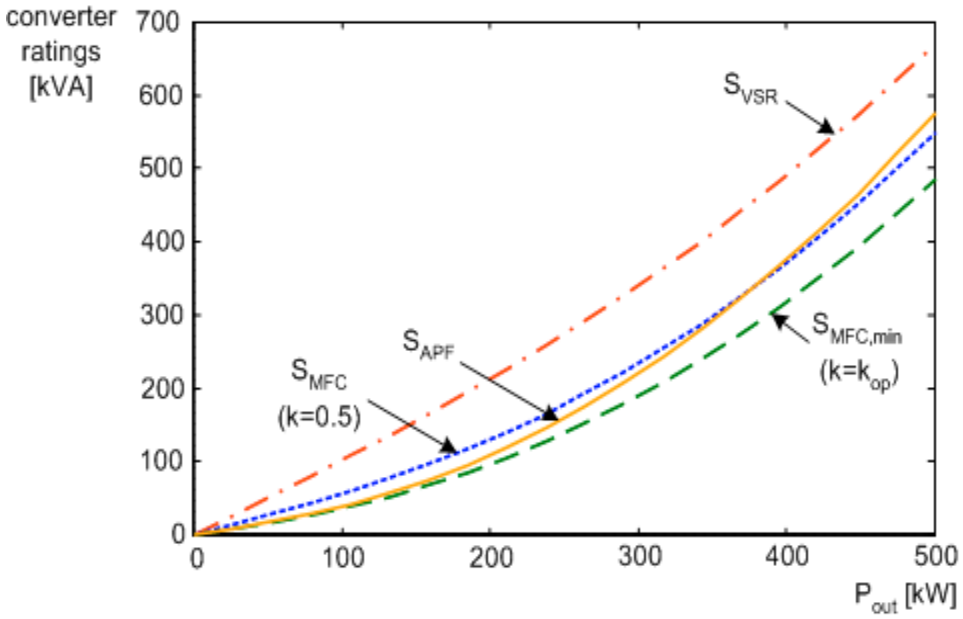


Fig. 5.13 Converter ratings versus output power and k (V_{LL}=460V, n=16, and L_s=3mH).

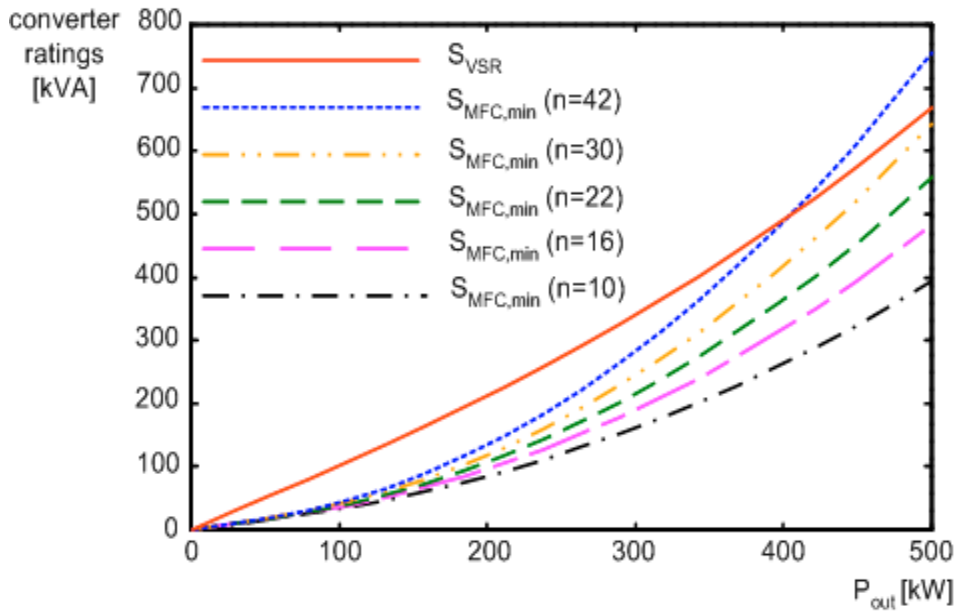


Fig. 5.14 Converter ratings as a function of output power and n (V_{LL}=460V and L_s=3mH).

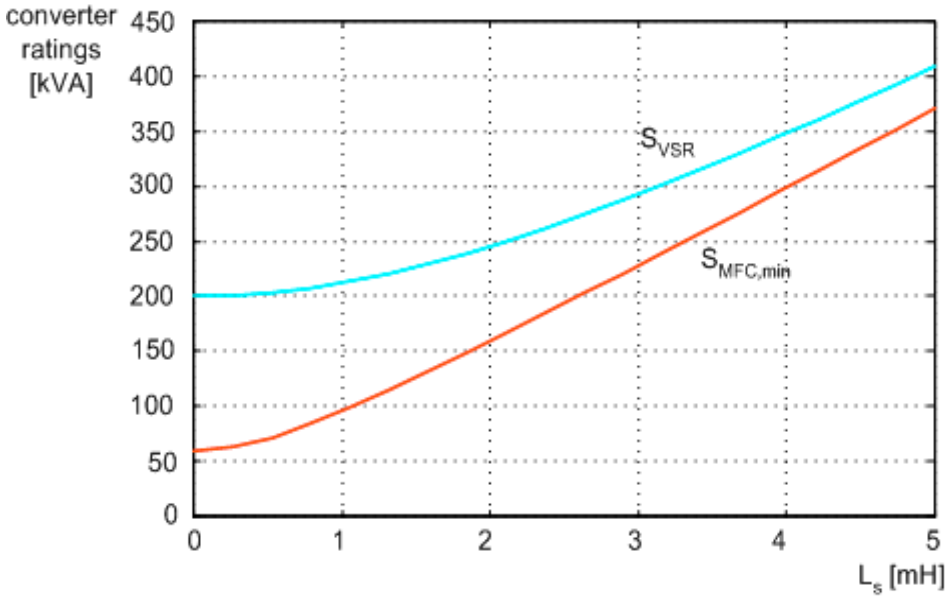


Fig. 5.15. Converter ratings versus input filter inductance (V_{LL}=460V, n=16, and P_{out}=300kW).

It is important to note that the minimum MFC rating ($S_{MFC,min}$) with the optimized split factor is lower than the APF rating (S_{APF}) for all output power ranges. Figure 5.14 shows a plot of the VSR rating and the minimum MFC ratings with several different n values versus output power with V_{LL}=460V and L_s=3mH. The minimum MFC rating increases with the increase of harmonic components number n which the MFC cancels, since the MFC should generate higher harmonic powers to obtain a supply current with less THD_{is}. Several n values (10, 16, 22, 30 and 42) used in Fig. 5.14 result in THD_{is} of 10, 8, 7, 6 and 5% in the supply current, respectively. Note that the minimum MFC rating with large number n may be higher than the VSR rating in high power applications.

Figure 5.15 shows the minimum MFC rating and the VSR rating as a function of the size of input inductor. It is shown that the MFC rating is more sensitive to the increase of input filter inductance than the VSR rating. This is because the input filter of the VSR is subject to the supply current with the fundamental frequency of 60 Hz, whereas the harmonic currents with higher frequencies flow through the input inductor of the MFC. As a result, the MFC input inductor has the higher reactance than the VSR

inductor with the same inductance. The economical aspect regarding the converter size, which is in favor of the MFC in low and medium power ranges, may change for high power applications, especially with the large input inductor and the diode rectifier with high harmonic current components.

5.3 DC-link voltage levels

Since both the VSR and the MFC have basically the same circuit configuration, the required dc-link voltage level for both of them can be determined based on the peak voltage on the ac side of the converters. The normal dc-link voltage for the VSR and the MFC is set at 5% higher than the peak line-to-line voltage across the converter ac side, assuming the maximum modulation index for the converters is 0.95 [56]. Therefore, the peak converter voltage on the ac side is the key factor to design the dc-link voltage level.

Since the supply voltage and the current are assumed purely sinusoidal, the input voltage of the VSR, u_s is simply modeled by the supply voltage and the voltage drop across the filter inductor.

$$u_s(\omega t) = v_s(\omega t) - \omega L_s \left(\frac{di_s(\omega t)}{d(\omega t)} \right) \tag{5.21}$$

Reflecting (5.1) to (5.21), the peak input voltage of the VSR, $u_{s,peak}$, is then calculated, under the unity power factor condition, as

$$u_{s,peak} = \sqrt{2} V_s \sqrt{1 + \left(\frac{\omega L_s P_{out}}{3 {V_s}^2} \right)^2} \tag{5.22}$$

This implies that the higher dc-link voltage level is required for applications with a large filter inductor or in high power applications.

The derivation of the MFC input voltage u_m is more complicated because the MFC input current includes harmonic components [61]. The input voltage on the MFC ac side with the parameters used in the previous analysis can be likewise derived, using (5.18), as

$$u_m(\omega t) = \sqrt{2}V_s\left[\cos\omega t + \frac{\omega L_s P_{out}}{3V_s^{\,2}}\sin\omega t\left\{(1-k)-2k\left(\sum_{m=1}^{n/2}\cos(6m\omega t)\right)\right\}\right] \quad (5.23)$$

Figure 5.16 shows the input voltage waveform on the MFC ac side for two output power split factors. The peak voltage value of the VSR under the same conditions is also included for comparison. The input voltages of the MFC ac side have sudden voltage spikes at every commutation instant of the corresponding phase current of the diode rectifier. Note that ideal current commutations in the diode rectifier are assumed with infinite di_L/dt. In practice, the diode rectifier current will be trapezoidal and the voltage spike level will be lower than that of Fig. 5.16. In some applications, additional input inductors on the diode rectifier are implemented to reduce the current slope and the resultant voltage spikes on the MFC ac side during the diode rectifier commutations. The effect of the input inductors on the diode rectifier is not dealt with in this analysis.

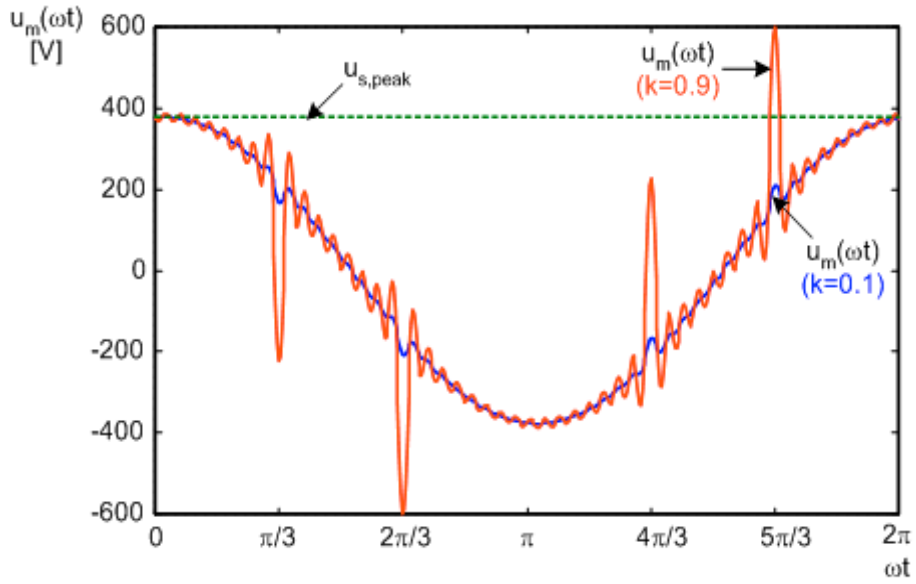


Fig. 5.16 MFC ac side voltages (V_{LL}=460V, L_s=0.5mH, P_{out}=100kW, and n=16).

The voltage spike at the commutation instant is exacerbated with higher inductance L_s and more output power through the diode rectifier (the higher k). Therefore, it can be deducted that the peak value of u_m occurs at the moment of either

ωt=0 or the commutation instant of the diode rectifier current according to constraints of P_{out}, L_s, k, and n. The condition is derived by

$$u_{m,peak} = \begin{cases} \sqrt{2}V_s & , if\ P_{out}\left[k(1+n)-1\right] \le \dfrac{\sqrt{3}V_s^{\,2}}{\omega L_s} \\ \sqrt{2}V_s\left[\dfrac{1}{2}+\dfrac{\sqrt{3}}{2}\dfrac{\omega L_s P_{out}}{3V_s^{\,2}}\{k(1+n)-1\}\right] & , if\ P_{out}\left[k(1+n)-1\right] \ge \dfrac{\sqrt{3}V_s^{\,2}}{\omega L_s} \end{cases} \tag{5.24}$$

The peak value of the MFC ac side yields $\sqrt{2}\,V_s$ which occurs at ωt=0 in low power applications, while the MFC peak voltage on the ac side occurs at commutation instant in high power levels. Theoretically, the dc-link voltage level should be set to a higher value than the ac side line voltage of the MFC at all times, including the commutation instants. However, in practical case, the nominal reference dc-link voltage for the APF or the MFC is designed by neglecting the commutation effect, since the high voltage spikes at commutation points lead to high dc-link voltage requirement, which yields high switch losses and cost. As an example, with supply line rms voltage V_{LL} of 460 V, the typical dc-link voltage of the MFC or the APF is set to 683 V by taking the peak ac side voltage at ωt=0 [46]. If this dc-link voltage is lower than the required voltage at commutation instants, the MFC loses current controllability at every instant of diode rectifier current commutation, resulting in a notch in the supply current. This will yield the deterioration in supply current quality though it can be permissible in low and medium power applications.

Figure 5.17 shows peak values of the ac side input voltages in the converters as a function of the total output power and k. As seen from Fig. 5.17, the peak input voltages for all converters are equal in the low power range. However, they increase nearly linearly with increasing output power in high power ranges. The increasing slopes of the curves in the MFCs are proportional to the power split factor k. Note that the slopes for all converters in Fig. 5.17 will increase if a bigger size L_s is used. Thus, in high power levels, the peak voltages of the MFCs are higher than that of the VSR, resulting in the theoretical requirement for a higher dc-link voltage level. High dc-link voltage results in

high switch losses and cost penalty. The case of the APF is the worst. It is to be noticed that the MFC with high k is not suitable for high power applications due to its high dc-link voltage requirement.

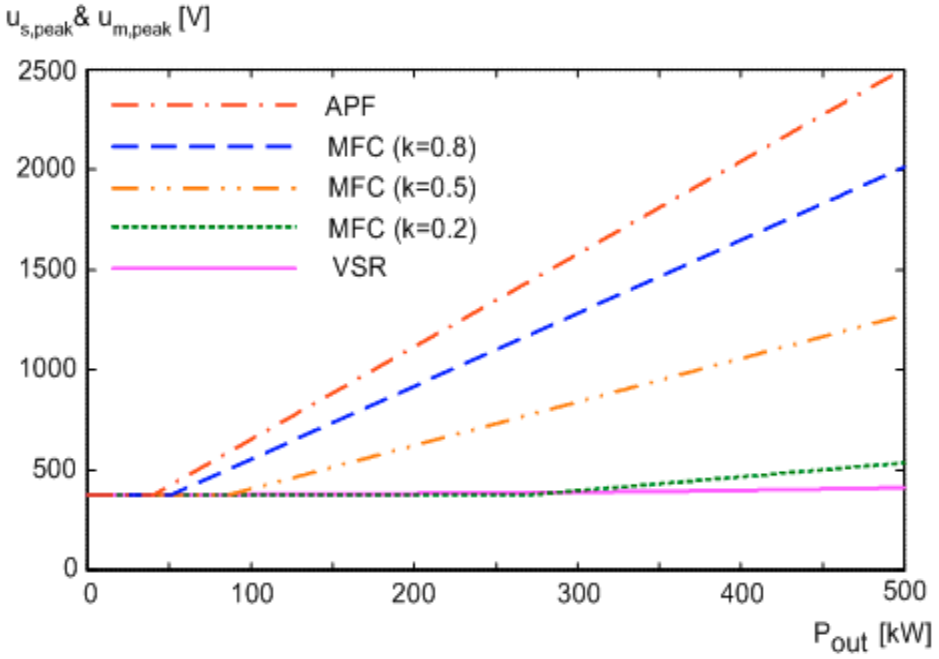


Fig. 5.17 Peak voltages on the ac side of converters versus output power and k (V_{LL}=460V and L_s=0.5mH).

5.4 Switch ratings

The mean and rms switch currents are found by integrating the positive input current of the converters and its square value over one supply cycle, respectively [59]. The mean switch current, the rms switch current, and the peak switch current for the VSR are related with the supply voltage and the total output power as

$$I_{sw,mean\,(VSR)} = \frac{\sqrt{2}}{3\pi}\frac{P_{out}}{V_s},\quad I_{sw,rms\,(VSR)} = \frac{1}{3\sqrt{2}}\frac{P_{out}}{V_s},\quad I_{sw,peak\,(VSR)} = \frac{\sqrt{2}}{3}\frac{P_{out}}{V_s} \qquad (5.25)$$

Since the shape of the MFC input current i_m varies by the power split factor k, the mean switch current of the MFC is also different by the split factor. The mean switch current is derived, according to k, by

$$I_{sw,mean(MFC)} = \begin{cases} \dfrac{\sqrt{2}P_{out}}{3V_s}\left(\dfrac{1}{\pi} - \dfrac{\pi}{6\sqrt{3}}k\right) & ,if\ 0 \le k \le \dfrac{\sqrt{3}}{\pi} \\ \dfrac{\sqrt{2}P_{out}}{3V_s}\left\{\dfrac{2}{\pi}\sin\theta_0 + \dfrac{k}{\sqrt{3}}\left(\dfrac{\pi}{6} - \theta_0\right) + \dfrac{1-\sqrt{3}}{\pi}\right\}, if\ \dfrac{\sqrt{3}}{\pi} \le k \le 1 \end{cases} \quad (5.26)$$

where, $\theta_0 = \cos^{-1}\left(\dfrac{\pi k}{2\sqrt{3}}\right)$

The rms switch current can be calculated as

$$I_{sw,rms(MFC)} = \frac{P_{out}}{3V_s}\sqrt{\frac{1}{2} + k\left\{\left(\frac{\pi}{3\sqrt{2}}\right)^2 k - 1\right\}} \quad (5.27)$$

The peak switch current is likewise found by split factor k:

$$I_{sw,peak(MFC)} = \begin{cases} \dfrac{\sqrt{2}P_{out}}{3V_s}\left(1 - \dfrac{\pi}{2\sqrt{3}}k\right) & ,if\ 0 \le k \le \dfrac{\sqrt{3}}{\pi} \\ \dfrac{P_{out}}{3\sqrt{2}V_s} & ,if\ \dfrac{\sqrt{3}}{\pi} \le k \le 1 \end{cases} \quad (5.28)$$

The peak switch current for the VSR and the MFC is important to design the dc-link capacitors, which is investigated in the next section. Figure 5.18 shows switch current ratios of the MFC and the VSR as a function of k. It is noticed that all MFC switch ratings are lower than those of the VSR over all power split factor. Since the MFC has lower current ratings and equal voltage ratings if the same dc-link voltage level is used for the VSR, it leads to better switch utilization for the MFC.

From the above analysis for switch currents for the two systems, approximate average switch power can be found by assuming equal switching loss proportional to the mean switch current and conduction loss in proportion to the rms switch current [59]. The average switch power is given, using the assumptions, by

$$P_{sw} = V_{sw,peak}\frac{I_{sw,mean} + I_{sw,rms}}{2} \quad (5.29)$$

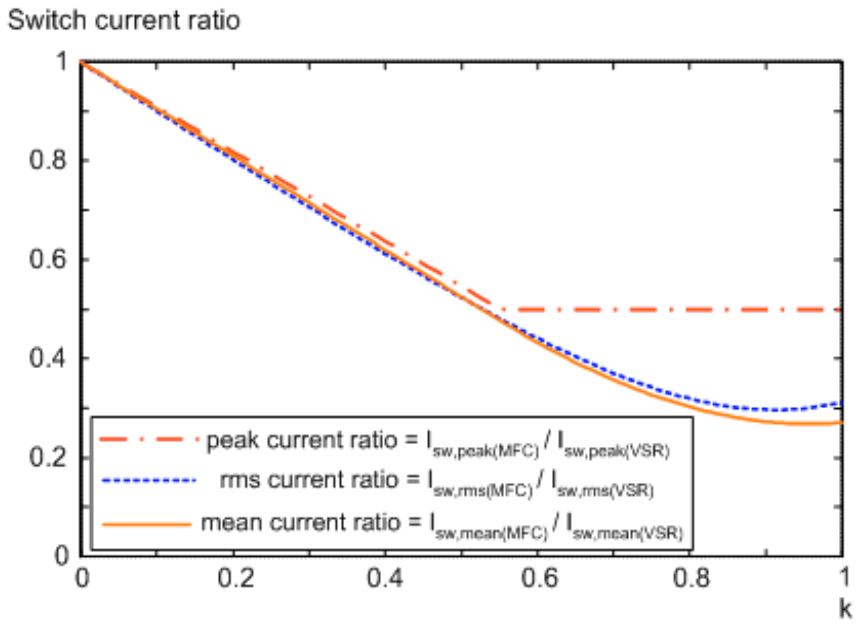


Fig. 5.18 Switch current ratios of the MFC and the VSR versus the split factor.

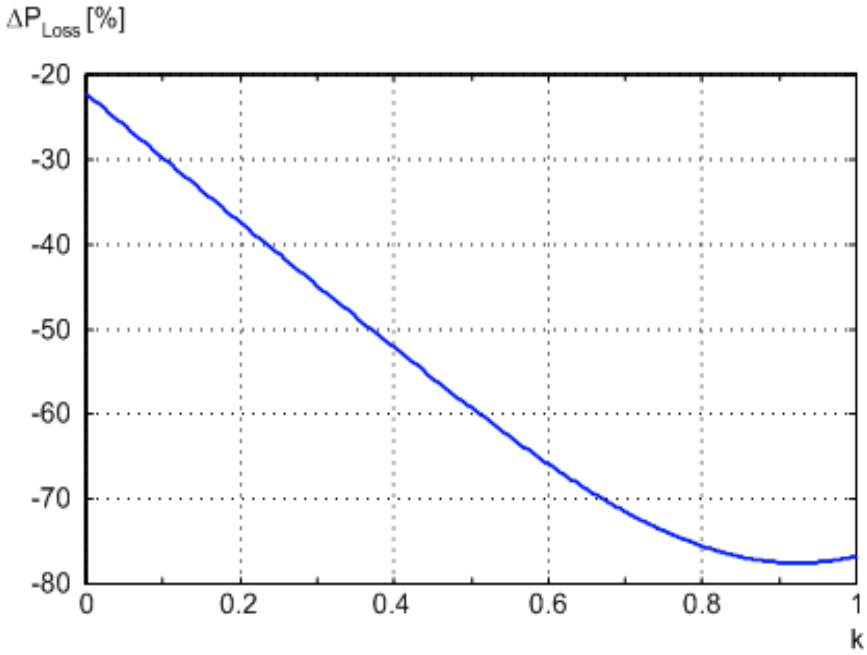


Fig. 5.19 Percent loss difference versus *k*.

One important criterion is the semiconductor loss performance of the VSR versus the MFC in actual applications. An index of the semiconductor loss difference ΔP_{Loss} is defined by

$$\Delta P_{Loss} = \frac{P_{sw(MFC)} - P_{sw(VSR)}}{P_{sw(VSR)}} \times 100\% \tag{5.30}$$

Notice that the loss difference depends only on the output power split factor k, by assuming that the two converters have the same dc-link voltage resulting in the same peak switch voltages. Figure 5.19 shows the semiconductor loss difference ΔP_{Loss} as a function of the power split factor. The MFC clearly features lower switching losses. This is due to only partial output powers flown through the MFC in comparison to the whole output power going through the VSR.

5.5 Reactive component ratings

Both the VSR and the MFC require an input filter inductor on the ac side that shapes the input currents and a dc-link capacitor on the dc side for energy storage.

5.5.1 Input filter inductance

Peak ripple current through the input inductor is chosen as a criterion to design the input filter inductor. In order to calculate the ripple current, the no-load condition is considered and the effect of inductor resistance is assumed to be negligible. Under these conditions, the inductance value is given by [36],

$$L_s = \frac{V_s}{2\sqrt{6}\, f_s\, i_{ripple,peak}} \tag{5.31}$$

where, f_s is the switching frequency and $i_{ripple,peak}$ denotes the allowed peak ripple current through the inductor. Since the same supply voltage is applied to the VSR and the MFC,

it is expected that two converters operating with the same switching frequency require an equal input inductor value with given identical peak ripple current constraint.

5.5.2 DC-link capacitance

The minimum capacitance value can be designed to limit the dc-link voltage ripple to a specified value, typically 1 to 2%. Thus, the peak to peak ripple voltage of the dc capacitor is adopted as a design criterion for the dc-link capacitor size.

5.5.2.1 VSR

With the assumption of a balanced three-phase utility system and neglecting the losses by the power switches, the VSR in the dc-link can be modeled as

$$C_{dc}\frac{dv_{dc}}{dt}=\sum_{\delta=1}^{3}i_{s\delta}d_{\delta}-\frac{P_{out}}{v_{dc}} \tag{5.32}$$

where, d_δ (δ=1,2,3) are switching functions. By noting that the first term of the right-hand in (5.32) is equal to one of the VSR input currents at all times, the possible maximum ripple voltage Δv_{dc} is obtained with the negative peak value of the VSR input current and 50% duty ratio [58]. For given allowable peak ripple voltage of Δv_{dc} and switching frequency, the capacitor value of the VSR is

$$C_{dc(VSR)}=P_{out}\frac{\sqrt{2}+3V_s/V_{dc}}{6\Delta v_{dc}V_s f_s} \tag{5.33}$$

where, V_{dc} is the desired level of the dc-link voltage.

5.5.2.2. MFC

The capacitor size of the MFC is likewise designed based on the peak input current of the MFC. Based on the MFC peak input current derived in (5.28), the capacitor value in the MFC is given by

$$C_{dc(MFC)} = \begin{cases} P_{out}\dfrac{\sqrt{2}(1-\pi k/2\sqrt{3})+3(1-k)V_s/V_{dc}}{6\Delta v_{dc}V_s f_s}, & if\ 0 \le k \le \dfrac{\sqrt{3}}{\pi} \\ P_{out}\dfrac{(1/\sqrt{2})+3(1-k)V_s/V_{dc}}{6\Delta v_{dc}V_s f_s}, & if\ \dfrac{\sqrt{3}}{\pi} \le k \le 1 \end{cases} \tag{5.34}$$

Figure 5.20 shows a minimum capacitance ratio, defined by (5.35), of two converters as a function of output power split factor.

$$\chi_1 = \frac{C_{dc(MFC)}}{C_{dc(VSR)}} \tag{5.35}$$

Note that the ratio depends only on the power split factor k assuming that the two converters operate with the same dc-link voltage. It can be seen that the dc-link capacitor size of the MFC is smaller than that of the VSR. This is due to the different power components dealt by the two converter capacitors. All real output power with dc components is supplied through the VSR capacitor. On the other hand, the MFC provides the partial real output power less than the total output power to its own load. Furthermore, the reactive and harmonic powers with higher frequency components through the MFC capacitor lead to smaller voltage variation than real power components.

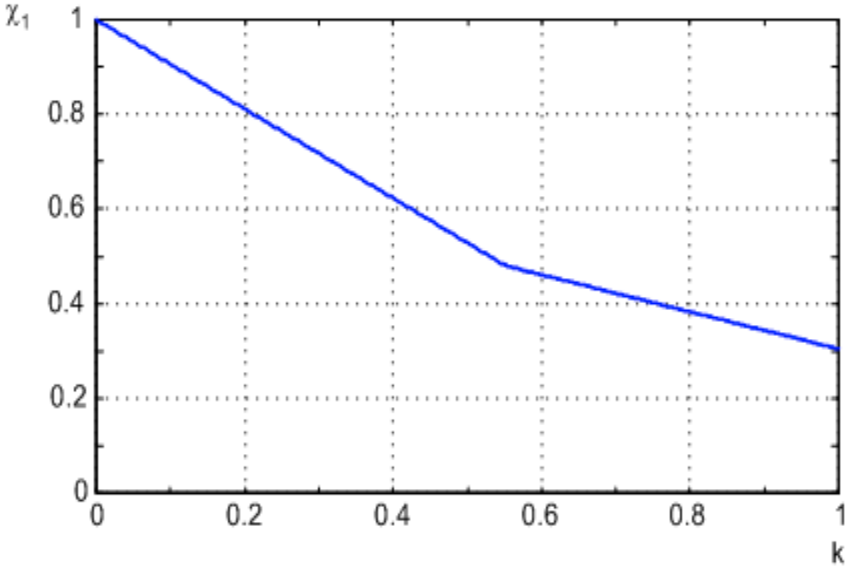


Fig. 5.20 Minimum capacitance ratio of two converters versus power split factor.

While the topology based on the VSR has only one dc-link capacitor, the counterpart using the MFC and the diode rectifier requires two capacitors for each rectifier. The capacitor value in the diode rectifier in Fig. 5.2, is given by [62]

$$C_{dc(diode)} = P_{out} \frac{\pi^2 k}{54\sqrt{6} f_g V_s \Delta v_{dc}} \tag{5.36}$$

The capacitor size on the diode rectifier is much larger than that of the VSR or the MFC, given the same ripple voltage requirement, since the former operates with the grid frequency f_g while the latter with the switching frequency f_s which is much faster than the grid frequency. Capacitance ratio of the two systems is defined by

$$\chi_2 = \frac{C_{dc(MFC)} + C_{dc(diode)}}{C_{dc(VSR)}} \tag{5.37}$$

Figure 5.21 shows a plot of capacitance ratio of the two systems with V_{LL} = 460V, V_{dc} = 683V, and f_s = 10kHz, given dc-link ripple voltage constraint. It is shown that the ratio linearly increases with the increasing split factor since the capacitance value of the diode rectifier is a dominant factor.

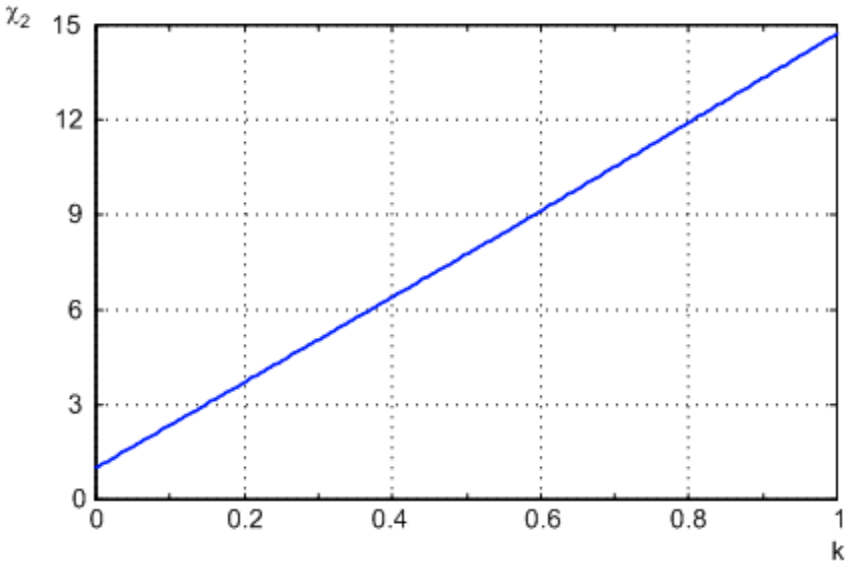


Fig. 5.21 Minimum capacitance ratio of the two systems versus the power split factor.

5.6 Conclusion

This chapter presents analytic design aspects and their systematical comparisons for the two converter systems based on the PWM-VSR and the MFC. The minimized MFC rating connected with a typical diode rectifier is more than 50% lower than the VSR rating in low and medium power applications. However, the difference in converter ratings is reduced as the output power increases, which means that the MFC loses its attractiveness of small size converter in high power applications. This situation is aggravated with a diode rectifier with more harmonic current components. Furthermore, the MFC rating shows higher sensitivity to the increase of input filter size than the VSR rating. Therefore, it can be concluded that the system combined with the MFC and the diode rectifier cannot be a better cost-effective solution in applications with a large input inductor and a diode rectifier at high distortion level, especially in high power areas.

The dc-link voltage levels for the MFC and the VSR are comparable in low and medium power areas. However, the MFC requires higher dc-link voltage level, leading to high switch loss and cost, due to the diode current commutation in high power level. This fact makes the MFC applications improper in high power areas, with the increasing converter rating. The MFC results in lower switch ratings for all conditions, leading to better switch utilization. The semiconductor loss of the MFC is also much lower than that of the VSR. Equal input inductance value can be used for both converters to comply with a given input peak current constraint. The dc-link capacitor value of the MFC is always smaller than that of the VSR. Notwithstanding the small size capacitor for the MFC, the total capacitor size of the MFC and the diode rectifier is about several times larger than the dc capacitor of the VSR due to big capacitor requirement of the diode rectifier given the same output voltage ripple constraint.

CHAPTER VI

CONCLUSIONS

6.1 Conclusions

In this dissertation, three-phase ac/ac power converters with specific superiority are addressed: a matrix converter to realize compact size converter, a current-fed converter with high-power handling capability, and converter type utility interface to obtain unity power factor. Based on the converter structures, this work designs and proposes new converter topologies and control algorithms to enhance their performance and provide solutions to conventional ones' drawbacks.

Various three-phase ac/ac power converters have been, in Chapter I, presented from most primitive structure with a PWM-VSI fed by a diode rectifier to matrix converter, current source inverters, PWM rectifiers, and active power filters. Topologies, operational principles, advantages, and drawbacks of each converter have been briefly reviewed with recent trends. Research objectives and dissertation outlines are included.

For the matrix converter, a new fault-tolerant PWM strategy has been proposed in Chapter II. Because matrix converter drives seek for most possible applications in aerospace and military areas where converter reliability is greatly important, the added fault-tolerant control would strengthen the matrix converter technology. When one of the matrix converter drive legs is completely lost, developed modulation strategy reshapes remaining output currents, resulting in continuous operation. The proposed add-on solution allows improved converter reliability with no converter structural modification as well as no hardware redundancy. Simulation and experimental results have been presented to demonstrate the feasibility of the proposed PWM strategy.

In Chapter III, a hybrid ac/ac power converter has been designed to realize high-performance system in high power applications. The proposed hybrid converter employs

a high-power load commutated inverter to provide real power and a medium-power voltage source inverter to generate reactive and harmonic powers to a load. Natural commutation of the load commutated inverter is achieved by the voltage source inverter, without any bulky and unreliable commutation capacitors and forced commutation circuits in conventional ones. The developed hybrid system ensures sinusoidal output current/voltage waveforms with high quality and fast dynamic response in high power areas, where a standalone voltage source inverter cannot apply due to its power limitation. Control method is also proposed to minimize power rating of the voltage source inverter. Loss performances and an alternative topology have been included. The feasibility of the proposed hybrid converter has been supported by computer simulation with a 500-hp induction motor and experimental results with a 1-hp induction motor.

A new topology and control scheme for a six-step current source inverter has been proposed in Chapter IV. The proposed topology utilizes small voltage source inverter, to turn off main thyristor switches, transfer reactive load energy, and limit peak voltages across loads. The control principle of the voltage source inverter is invented, resulting in very simple and reliable commutation processes. The VSI operates only during commutation periods of the load currents and stops working over the non-commutation intervals. Thus, the VSI with small power rating can be used for the proposed CSI system The proposed topology maximizes benefits of the constituent converters: high-power handling capability of large six-step current source inverters as well as fast and easy control of small voltage source inverters. The simulation and experimental results have verified the developed topology and control algorithm.

In Chapter V, this work has analyzed, compared, and evaluated two topologies for unity power factor with sinusoidal input currents and multiple ac/ac power conversions. From input and output terminal point of view, equal features are obtained through the two systems: single PWM rectifier with two inverter-load units, and the compound circuits of the diode rectifier and active power filter with its own inverter-load units. Thus, the theoretical analyses and systematic comparisons of the two topologies have been presented from the internal standpoint: converter kVA ratings, dc-

link voltage requirements, switch ratings, semiconductor losses, and reactive component sizes. Rigorous mathematical models for the two systems have been developed and obtained results have been used to evaluate the two converters under identical terminal constraints.

6.2 Suggestions for future work

Further investigation for the fault-tolerant matrix converter in Chapter II would continue for other types of system faults such as one-phase short-circuit fault. Theoretical analyses based on mathematical approaches in Chapter V could be also verified with simulation models to consider effects of actual circuit components.

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APPENDIX

DERIVATION OF EQUATIONS IN CHAPTER V

A. Derivation of (5.2)

The kVA rating of the VSR can be defined in terms of the rms voltage and the rms current on ac side of the VSR as

$$S_{VSR} = 3U_s^{rms} I_s \tag{A.1}$$

where, U_s^{rms} is the rms value of the input voltage of the rectifier, u_s. The rms value U_s^{rms} can be calculated by

$$U_s^{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left\{v_s(\omega t) - \omega L_s \frac{di_s(\omega t)}{d(\omega t)}\right\}} = \sqrt{V_s^2 + (\omega L_s I_s)^2} \tag{A.2}$$

With the assumption of unity power factor and no losses in the VSR and the inductor, the rms current is related to the output power as

$$I_s = \frac{P_{out}}{3V_s} \tag{A.3}$$

Reflecting (A.2) and (A.3) into (A.1), one can obtain (5.2).

B. Derivation of (5.7)

The rating of the diode rectifier is described, from Fig. 5.5, by

$$S_{diode\ rectifier} = \sqrt{P_2^2 + Q_2^2 + H_2^2} \tag{A.4}$$

Then, using (5.6) and (5.16), it can be written by

$$S_{diode\ rectifier} = \frac{P_2}{\cos\varphi_1}\sqrt{1 + THD_i^2} \tag{A.5}$$

Reflecting (5.6), (5.16), and (A.5) back to (5.3), the equation (5.7) is derived.

C. Derivation of (5.19)

The rms value of the diode rectifier current $I_{L,rms}$ is simply

$$I_{L,rms} = \sqrt{\frac{2}{3}} I_{dc} \tag{A.6}$$

By Fourier analysis, the dc-side current of the diode rectifier, I_{dc} is

$$I_{dc} = \frac{\pi}{\sqrt{6}} I_{s2} \tag{A.7}$$

By substituting (A.6), (A.7), and (5.16) into (5.15), one can obtain the MFC rms current value as

$$I_{m,rms}^2 = \frac{1}{9V_s^2}\left\{ P_1^2 - (1-\frac{\pi^2}{9}) P_2^2 \right\} \tag{A.8}$$

In addition, the rms voltage of the MFC, $U_{m,rms}^2$, can be expanded by substituting (5.1), (5.16), (5.18), and (A.7) into (5.17). Using the features of (A.9), it can be shortened to (A.10).

$$\begin{aligned} &\int_0^{2\pi} \cos(m\omega t)\cdot\sin(n\omega t)\cdot d(\omega t) = 0, \quad for \quad all \quad m, n \\ &\int_0^{2\pi} \sin(m\omega t)\cdot\sin(n\omega t)\cdot d(\omega t) = 0, \quad for \quad m \neq n \end{aligned} \tag{A.9}$$

$$U_{m,rms}^2 = V_s^2 + \left(\frac{\omega L_s}{3V_s}\right)^2 \left(P_1^2 + nP_2^2\right) \tag{A.10}$$

Finally, one can derive (5.19) by substituting (A.8) and (A.10) into (5.14).

D. Derivation of (5.23)

Similar to (5.21), the MFC input voltage on its ac side, u_m, is

$$u_m(\omega t) = v_s(\omega t) - \omega L_s \left(\frac{di_m(\omega t)}{d(\omega t)}\right) \tag{A.11}$$

Applying (5.1), (5.9), (5.16), (5.18), and (A.7) to (A.11), (A.11) can be solved. Using the feature (A.12), one can finally obtain (5.23)

$$\sin\alpha - \sin\beta = 2\cdot\cos\left(\frac{\alpha+\beta}{2}\right)\cdot\sin\left(\frac{\alpha-\beta}{2}\right) \tag{A.12}$$

E. Derivation of (5.24)

From Fig. 5.16, it can be seen that the peak value of $u_m(\omega t)$ occurs at the moment of either ωt=0 or the commutation instant of the diode rectifier current (ωt=5π/3), depending on P_{out}, L_s, k, and n. From (5.23), the MFC input voltage values at two instants are given by

$$u_m(\omega t) = \begin{cases} \sqrt{2}V_s & , \ if \ \ \omega t = 0 \\ \sqrt{2}V_s\left[\dfrac{1}{2} + \dfrac{\sqrt{3}}{2}\dfrac{\omega L_s P_{out}}{3{V_s}^2}\{k(1+n)-1\}\right] & , \ if \ \ \omega t = \dfrac{5\pi}{3} \end{cases} \tag{A.13}$$

By comparing the two values of (A.13), the peak values and conditions can be obtained as

$$u_{m,peak} = \begin{cases} u_m(\omega t = 0) & , \ if \ \ P_{out}\left[k(1+n)-1\right] \le \dfrac{\sqrt{3}{V_s}^2}{\omega L_s} \\ u_m(\omega t = \dfrac{5\pi}{3}) & , \ if \ \ P_{out}\left[k(1+n)-1\right] \ge \dfrac{\sqrt{3}{V_s}^2}{\omega L_s} \end{cases} \tag{A.14}$$

F. Derivation of (5.25)

The equation of (5.25) can be calculated using

$$I_{sw,mean(VSR)} = \frac{1}{\pi}\int_0^{\pi/2} |i_s(\omega t)| d(\omega t) \tag{A.15}$$

$$I_{sw,rms(VSR)} = \sqrt{\frac{1}{\pi}\int_0^{\pi/2} i_s^2(\omega t) d(\omega t)} \tag{A.16}$$

G. Derivation of (5.26)

The mean switch current of the MFC is likewise given by

$$I_{sw,mean(MFC)} = \frac{1}{\pi}\int_0^{\pi/2} |i_m(\omega t)| d(\omega t) \tag{A.17}$$

From Fig. 5.9, the MFC input current is

$$i_m(\omega t) = \begin{cases} i_s(\omega t) - I_{dc} & , if \ 0 \le \omega t \le \dfrac{\pi}{3} \\ i_s(\omega t) & , if \ \dfrac{\pi}{3} \le \omega t \le \dfrac{\pi}{2} \end{cases} \tag{A.18}$$

Using (5.1), (5.9), (5.16), (A.3), and (A.7) into (A.18), the MFC current is given by

$$i_m(\omega t) = \begin{cases} \dfrac{\sqrt{2}P_{out}}{3V_s}(\cos\omega t - \dfrac{\pi}{2\sqrt{3}}k) & , if \ 0 \le \omega t \le \dfrac{\pi}{3} \\ \dfrac{\sqrt{2}P_{out}}{3V_s}\cos\omega t & , if \ \dfrac{\pi}{3} \le \omega t \le \dfrac{\pi}{2} \end{cases} \tag{A.19}$$

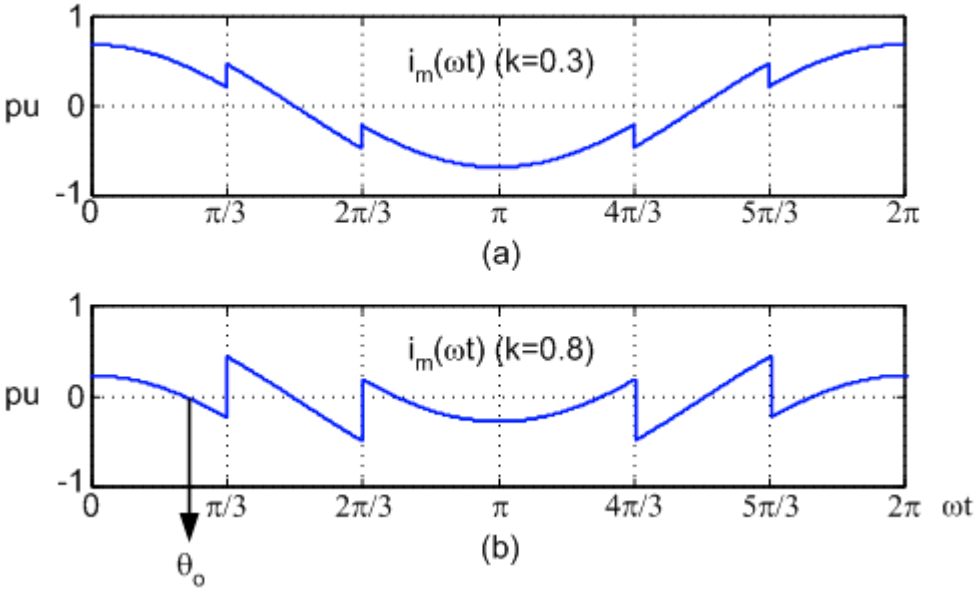

Fig. A.1. MFC input current waveforms (a) with k=0.3 (b) with k=0.8.

As seen in Fig. A.1, the shape of the MFC input current i_m varies by the power split factor k. Small k value in Fig. A.1(a) keeps the MFC input current positive during the entire quarter period from 0 to $\pi/2$. In case of large k at Fig. A.1(b), the instant θ_0, where i_m crosses to zero, can be found from (A.19)

$$\theta_0 = \cos^{-1}\left(\frac{\pi k}{2\sqrt{3}}\right) \tag{A.20}$$

Boundary condition of k, which Fig.A.1(b) is effective, is given by

$$0 \le \cos^{-1}\left(\frac{\pi k}{2\sqrt{3}}\right) \le \frac{\pi}{3} \tag{A.21}$$

This yields

$$\frac{\sqrt{3}}{\pi} \le k \le 1 \tag{A.22}$$

For k value less than $\sqrt{3}/\pi$, the mean switch current is found, as shown in Fig. A.1(a), by

$$I_{sw,mean(MFC)} = \frac{1}{\pi}\left[\int_0^{\pi/3} i_m(\omega t)d(\omega t) + \int_{\pi/3}^{\pi/2} i_m(\omega t)d(\omega t)\right] \tag{A.23}$$

For k value in (A.22), the mean switch current from Fig. A.1(b), is

$$I_{sw,mean(MFC)} = \frac{1}{\pi}\left[\int_0^{\theta_0} i_m(\omega t)d(\omega t) - \int_{\theta_0}^{\pi/3} i_m(\omega t)d(\omega t) + \int_{\pi/3}^{\pi/2} i_m(\omega t)d(\omega t)\right] \tag{A.24}$$

Solving two equations leads to (5.26).

H. Derivation of (5.28)

Considering the MFC input current waveforms with varying k, one can conclude that the peak value of i_m occurs at the instant of either ωt=0 or π/3. By comparing two values, $i_m(\omega t = 0)$ and $i_m(\omega t = \pi/3)$ using (A.19), one can derive (5.28).

VITA

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